SPP3407D
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3407D is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

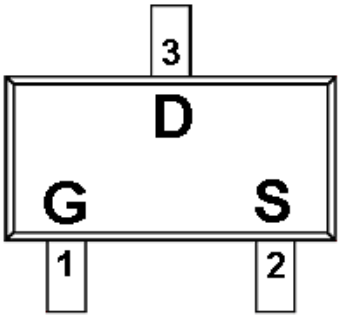
APPLICATIONS

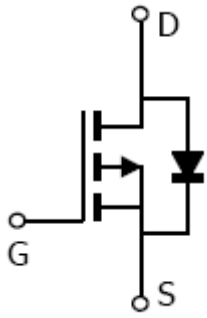
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

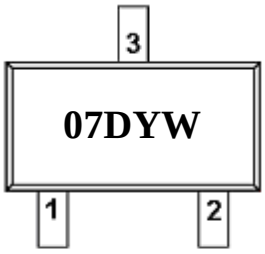
- -30V/-4.0A,$R_{DS(ON)}$=70mΩ@V_{GS}=-10V
- -30V/-3.2A,$R_{DS(ON)}$=95mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PIN CONFIGURATION(SOT-23)





PART MARKING



Y : Year Code
W : Week Code

SPP3407D
P-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3407DS23RGB	SOT-23	07D

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP3407DS23RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

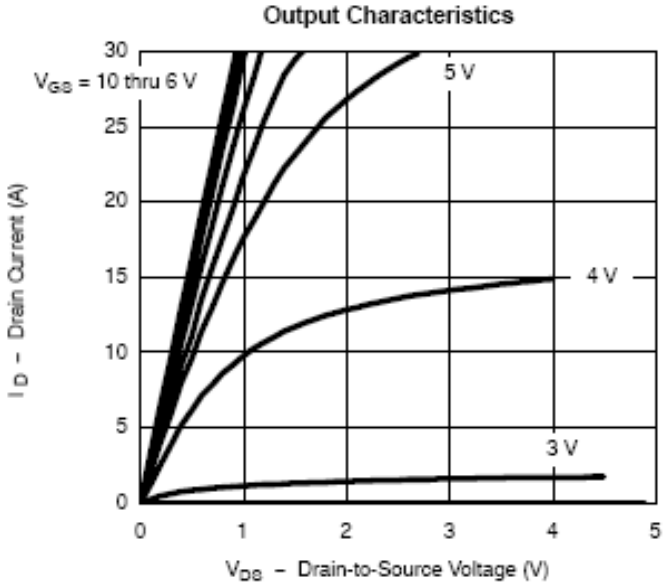
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150°C)	T_A=25°C	I_D	-3.6	A
	T_A=70°C		-3.0	
Pulsed Drain Current		I_{DM}	-15	A
Continuous Source Current(Diode Conduction)		I_S	-1.0	A
Power Dissipation	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Operating Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	°C/W

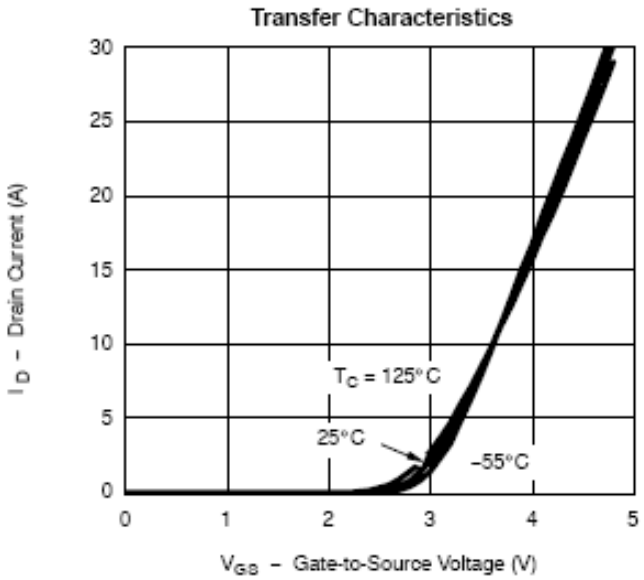
ELECTRICAL CHARACTERISTICS

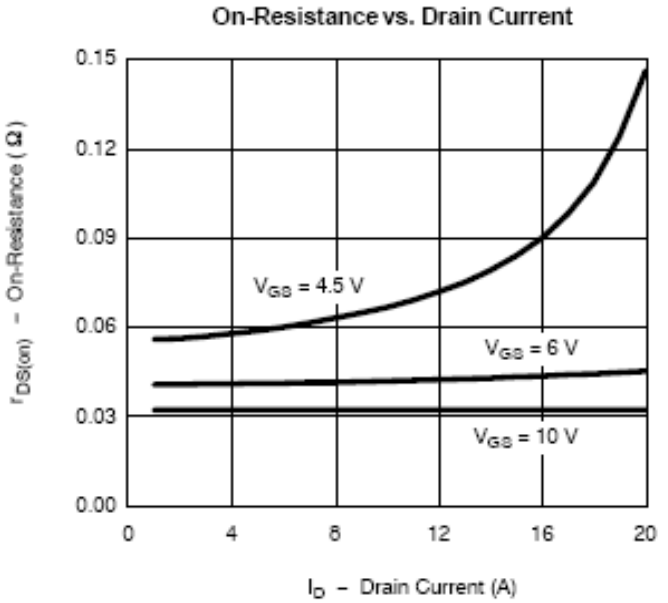
(T_A=25°C Unless otherwise noted)

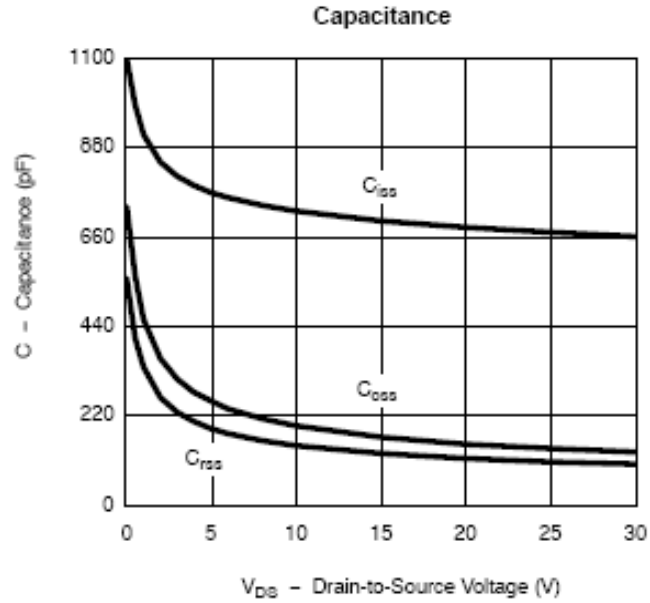
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.8		-2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_J=55°C			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-10V	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-4.0A		0.062	0.070	Ω
		V_{GS}=-4.5V,I_D=-3.2A		0.085	0.095	
Forward Transconductance	gfs	V_{DS}=-5.0V,I_D=-4.0A		10		S
Diode Forward Voltage	V_{SD}	I_S=-1.0A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V I_D= -3.5A		10	18	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		450		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			55		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω I_D≡-1.0A,V_{GEN}=-10V R_G=6Ω		8	18	nS
	t_r			8	18	
Turn-Off Time	$t_{d(off)}$			25	50	
	t_f			25	35	

TYPICAL CHARACTERISTICS









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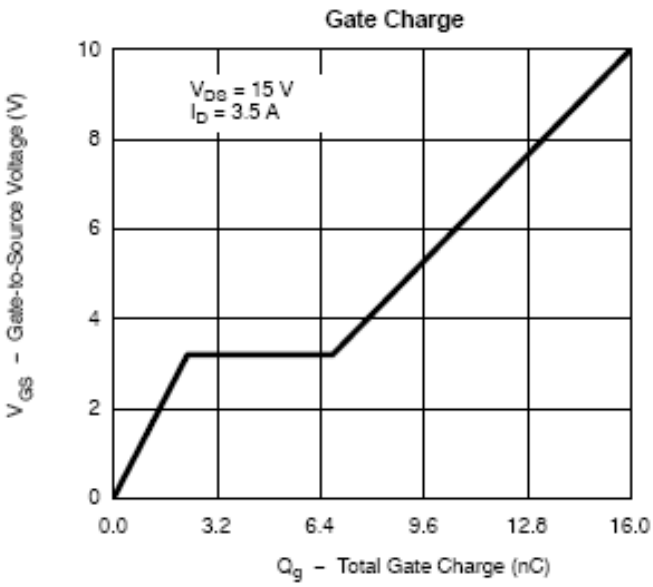

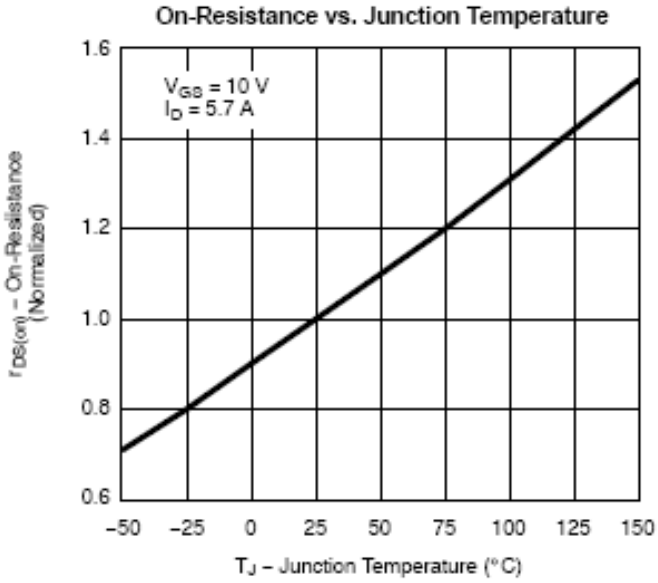

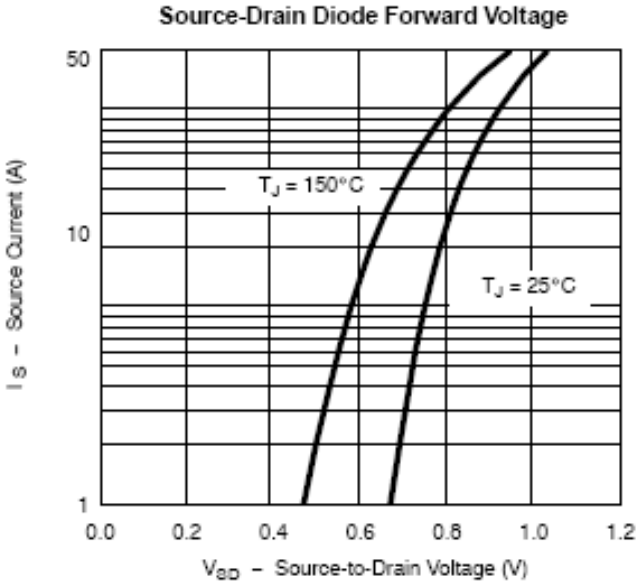

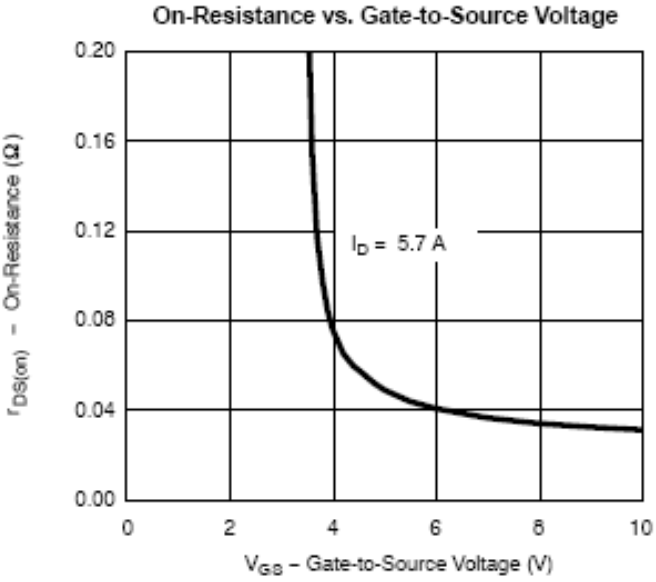

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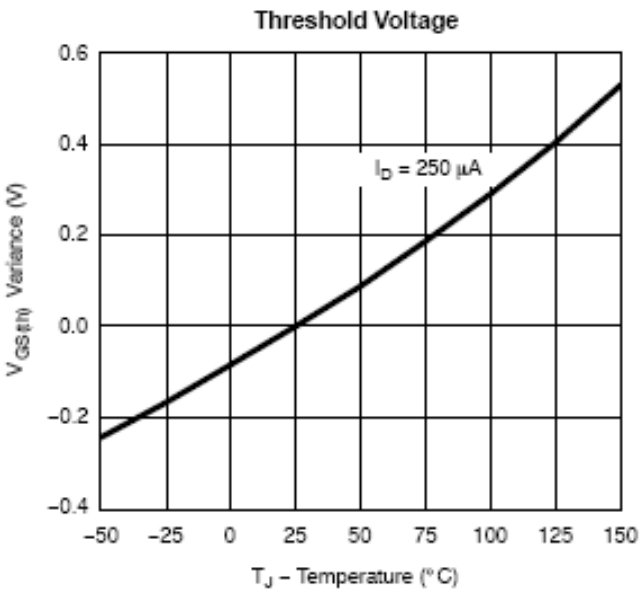

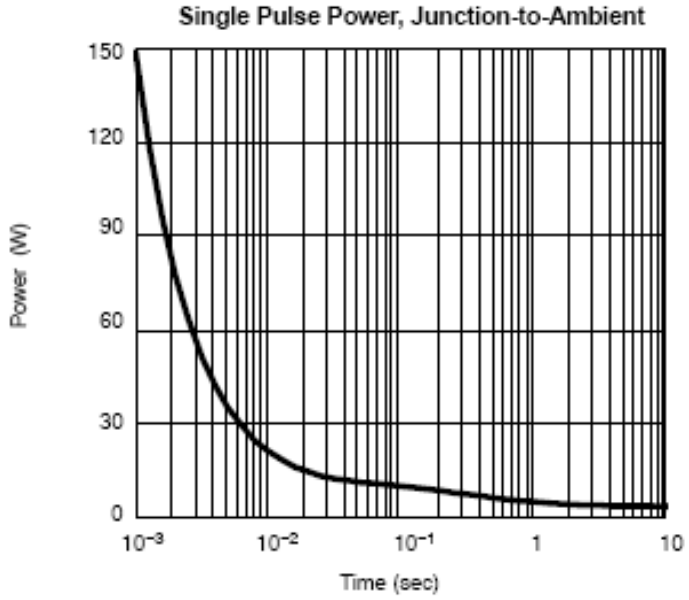

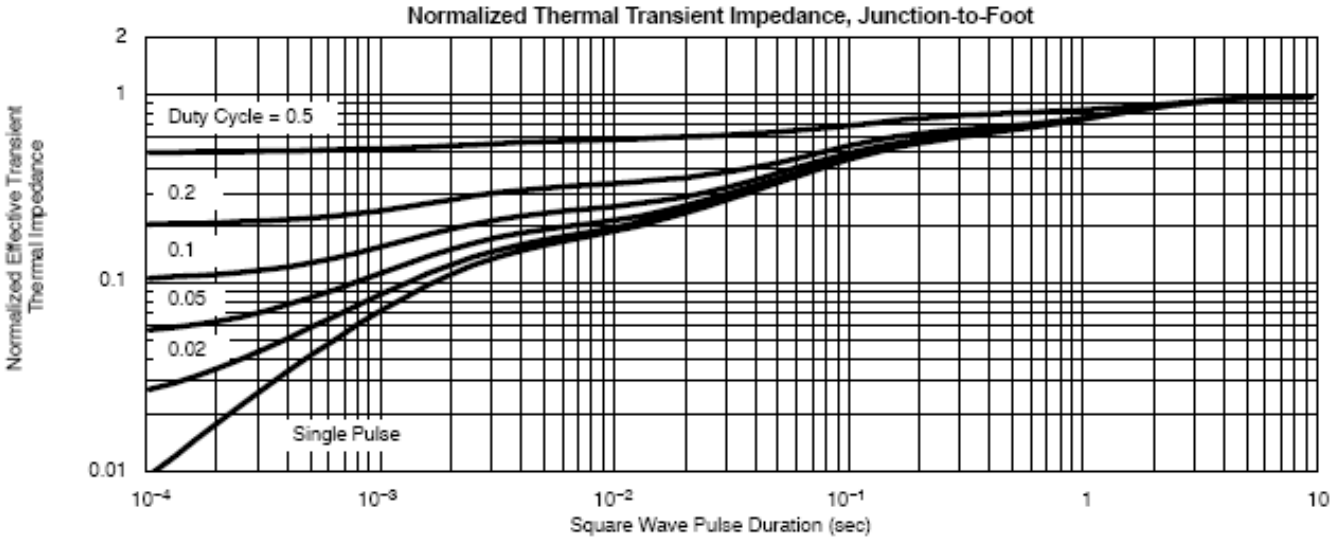

SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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