



SPP4437 P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP4437 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP4437 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

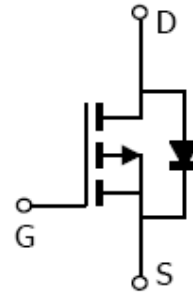
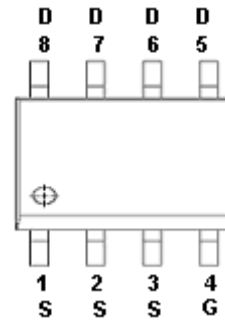
- ◆ -30V/-10A, $R_{DS(ON)}=8.5m\Omega@V_{GS}=-10V$
- ◆ -30V/-8A, $R_{DS(ON)}=14.5m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

APPLICATIONS

- MB/VGA/Vcore/PD Application
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

SOP-8



PART MARKING





SPP4437

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP4437S8RGB	SOP-8	SPP4437

※ SPP4437S8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-30	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current	I _D	TA=25°C	-13.5	A
		TA=70°C	-10.8	
Pulsed Drain Current	I _{DM}	-50	A	
Power Dissipation	P _D	TA=25°C	2.8	W
		TA=70°C	1.8	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient (t ≤ 10s)	R _{θJA}	70	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V, T_J=100^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq -5V, V_{GS}=-10V$			-100	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$		7	8.5	mΩ
		$V_{GS}=-4.5V, I_D=-8A$		11.4	14.5	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-3A$		14		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-4.5V$ $I_D=-10A$		35		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			10.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		3300		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			280		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V,$ $I_D=-1A, V_{GS}=-10V, R_G=6\Omega$		24.5		nS
	t_r			10.5		
Turn-Off Time	$t_{d(off)}$			156		
	t_f			50		



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TYPICAL CHARACTERISTICS

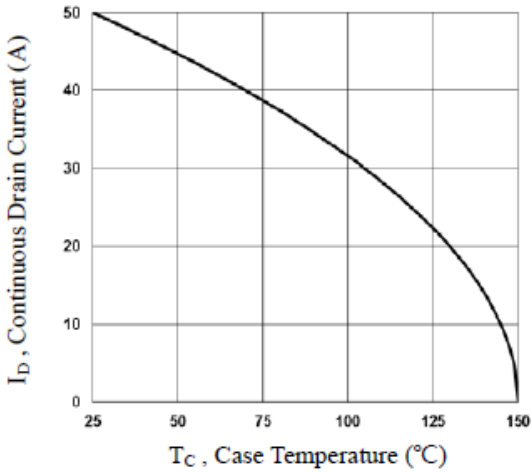


Fig.1 Continuous Drain Current vs. T_C

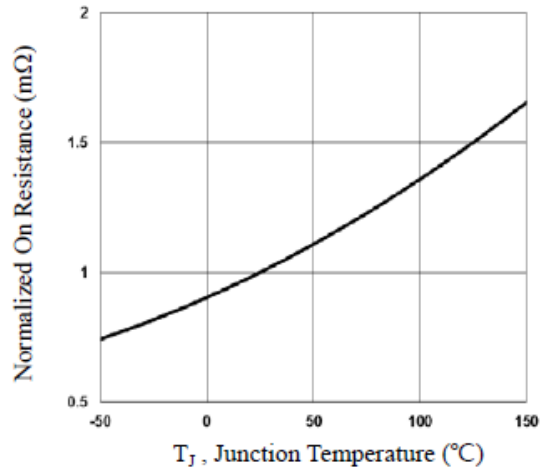


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

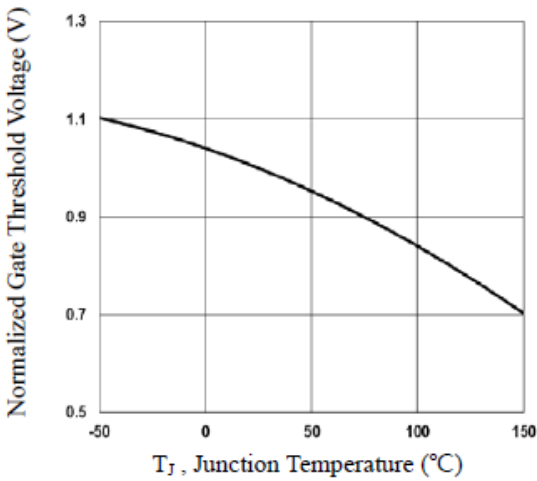


Fig.3 Normalized V_{th} vs. T_J

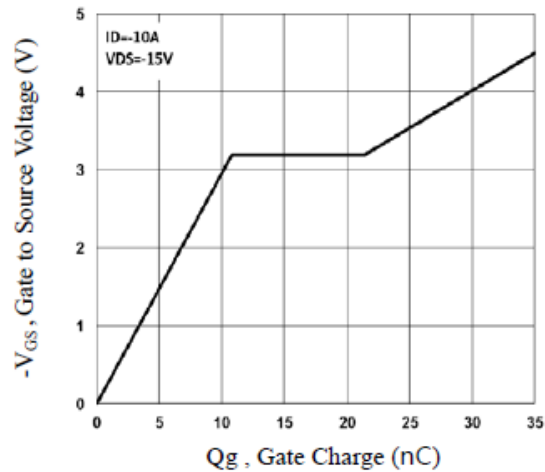


Fig.4 Gate Charge Waveform

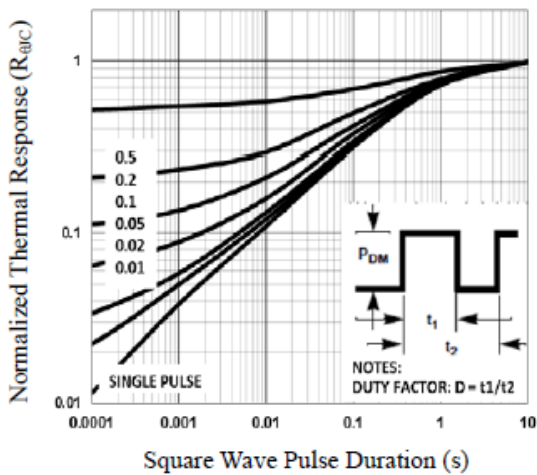


Fig.5 Normalized Transient Impedance

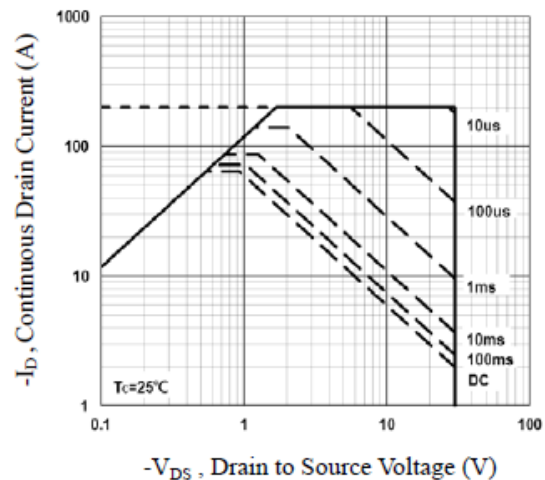


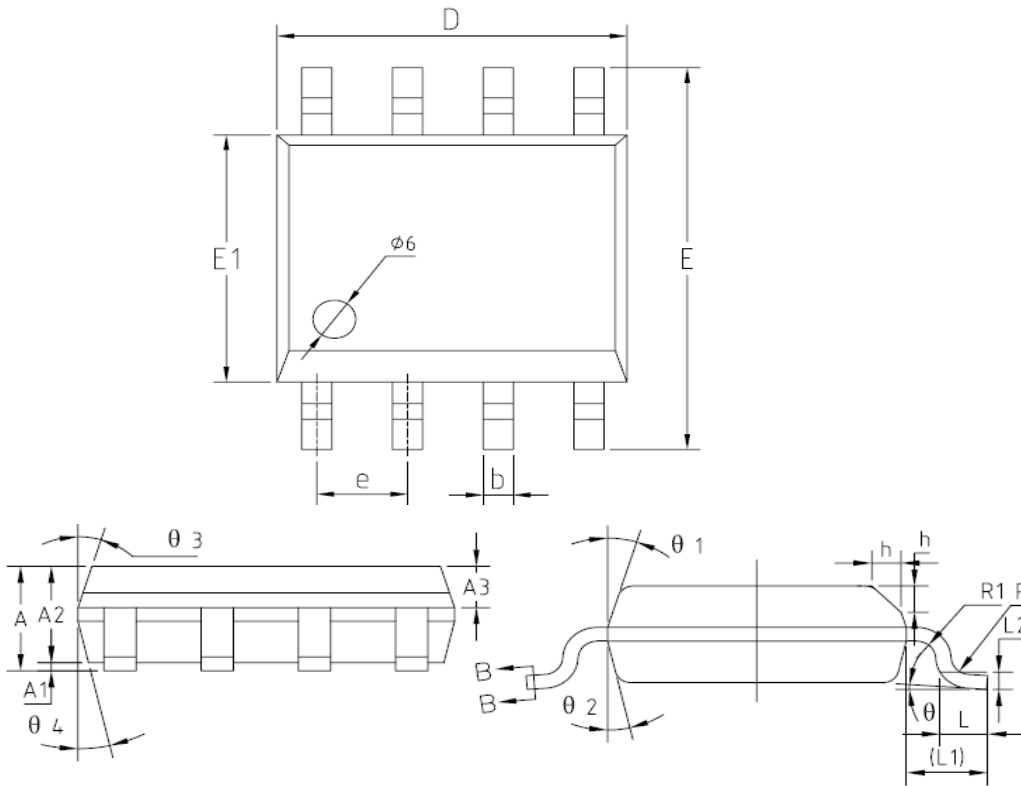
Fig.6 Maximum Safe Operation Area



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SOP-8 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.35	--	1.75
A1	0.10	--	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.33	-	0.51
c	0.17	--	0.25
D	4.80	4.93	5.05
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	0.20
h	0.25	--	0.50
θ	0°	--	8°
$\theta 1$	15°	17°	19°
$\theta 2$	11°	13°	15°
$\theta 3$	15°	17°	19°
$\theta 4$	11°	13°	15°



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