



SPP6309

Dual P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP6309 is the Dual P-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

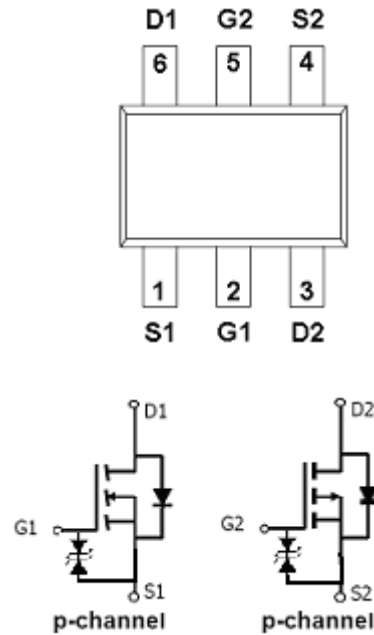
FEATURES

- ◆ P-Channel
 - 20V/0.45A, $R_{DS(ON)}=520m\Omega@V_{GS}=-4.5V$
 - 20V/0.35A, $R_{DS(ON)}=700m\Omega@V_{GS}=-2.5V$
 - 20V/0.25A, $R_{DS(ON)}=1500m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-363 (SC-70-6L) package design

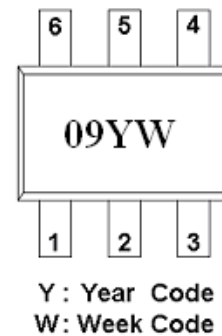
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-363/SC-70-6L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP6309S36RGB	SOT-363	09YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP6309S36RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-20	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-1.0
		TA=70°C	-0.7
Pulsed Drain Current	I _{DM}	-3	A
Continuous Source Current(Diode Conduction)	I _S	-0.6	A
Power Dissipation	P _D	TA=25°C	0.35
		TA=70°C	0.19
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	T ≤ 10sec	360
		Steady State	400



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ELECTRICAL CHARACTERISTICS

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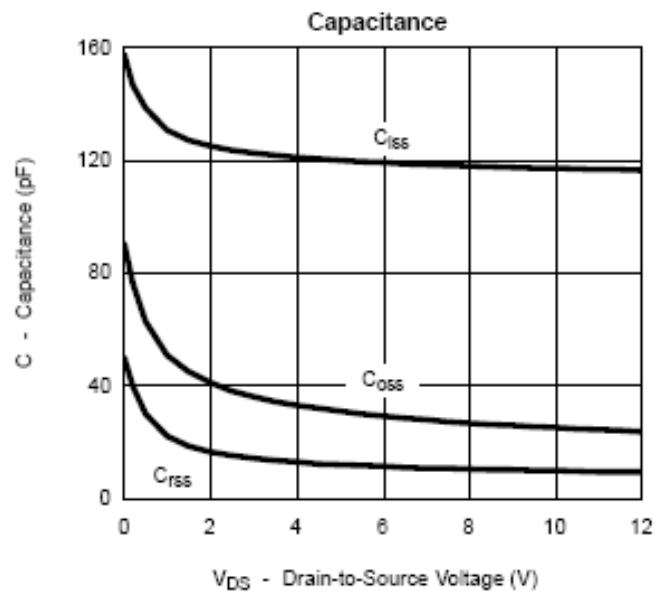
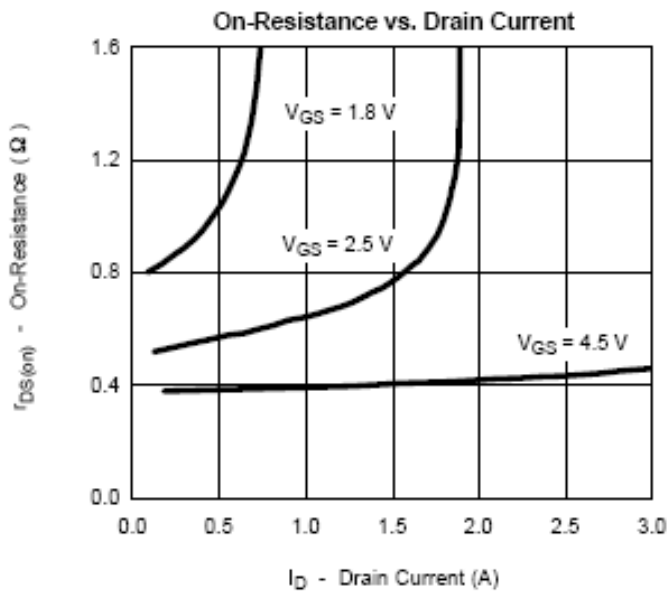
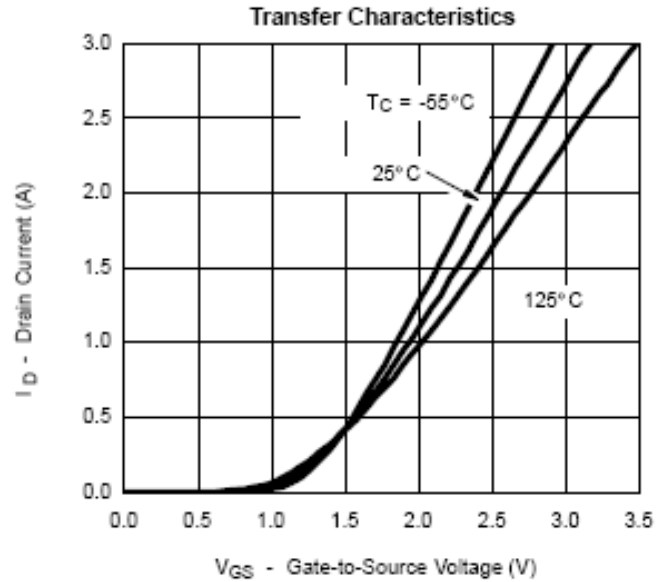
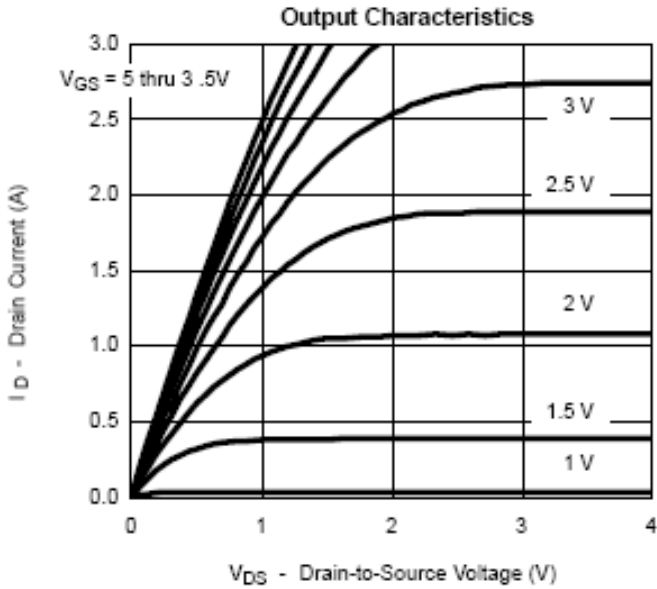
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -4.5V, V_{GS}=-5V$	-2			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-0.45A$		0.42	0.52	Ω
		$V_{GS}=-2.5V, I_D=-0.35A$		0.58	0.70	
		$V_{GS}=-1.8V, I_D=-0.25A$		0.95	1.5	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-1.0A$		1.5		S
Diode Forward Voltage	V_{SD}	$I_S=-0.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = -10V, V_{GS} = -4.5 V$ $I_D = -0.88 A$		1.5	2.0	nC
Gate-Source Charge	Q_{gs}			0.3		
Gate-Drain Charge	Q_{gd}			0.2		
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V$ $f=1MHz$		145		pF
Output Capacitance	C_{oss}			25		
Reverse Transfer Capacitance	C_{rss}			10		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=20\Omega,$ $I_D=-0.5A$ $V_{GEN}=-4.5V, R_G=6\Omega$		18	30	ns
	t_r			25	40	
Turn-Off Time	$t_{d(off)}$			15	45	
	t_f			12	20	



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TYPICAL CHARACTERISTICS

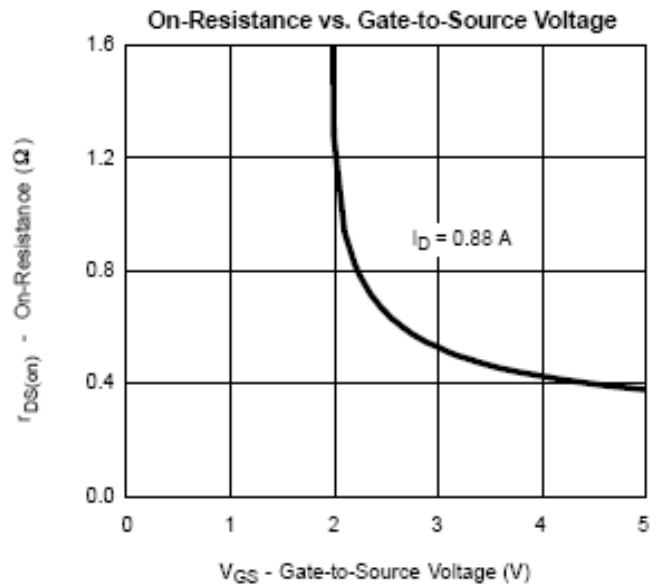
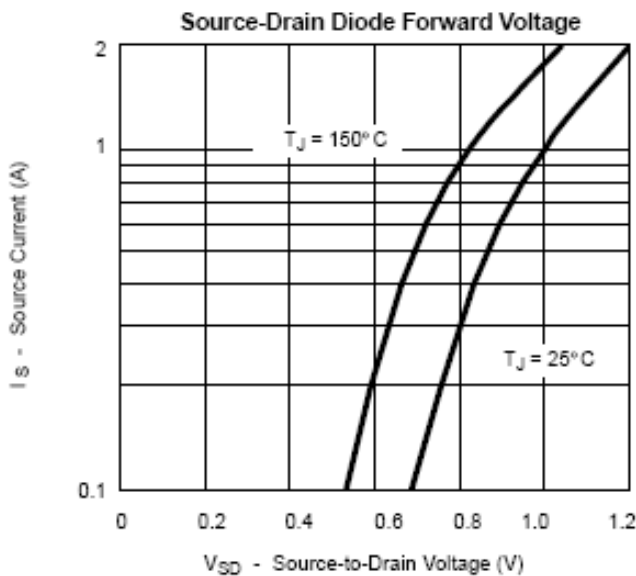
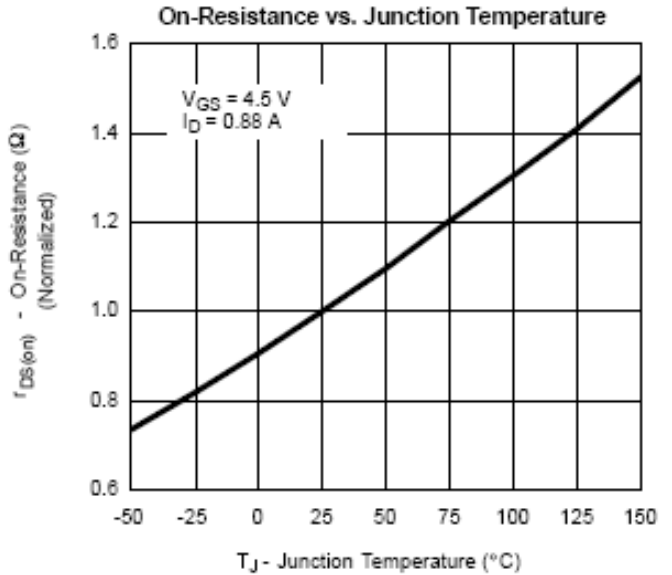
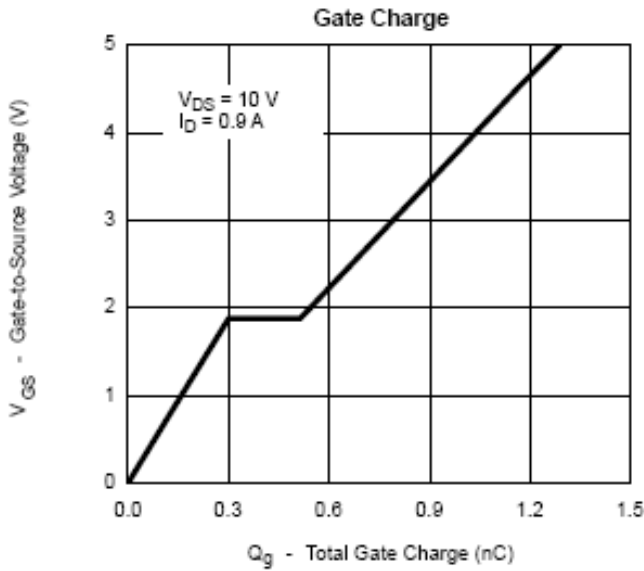




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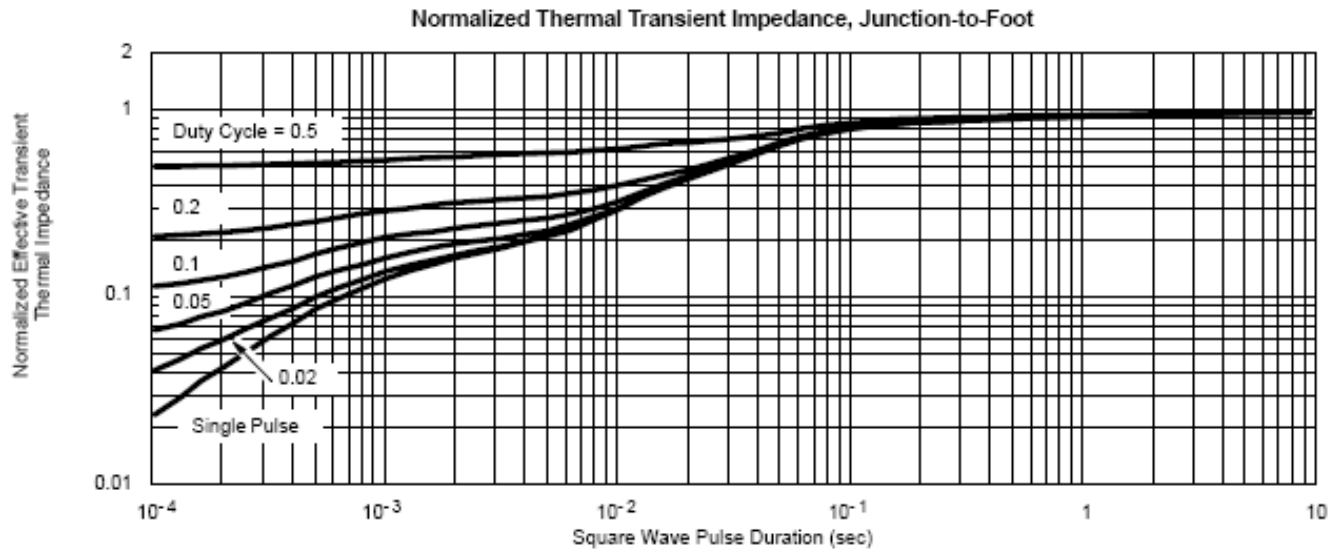
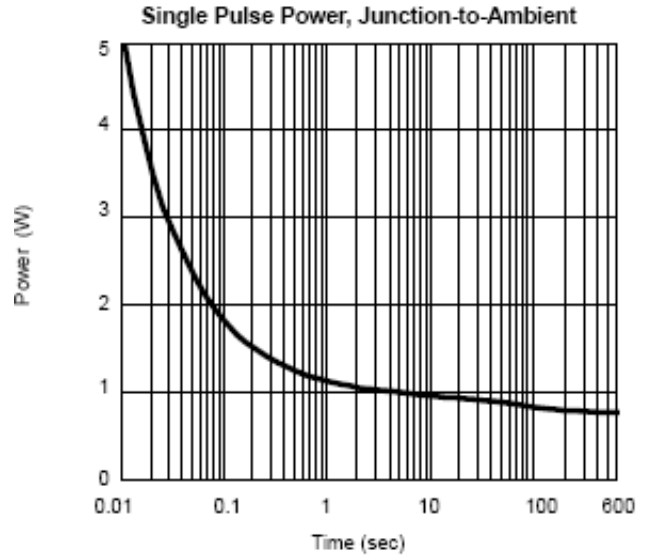
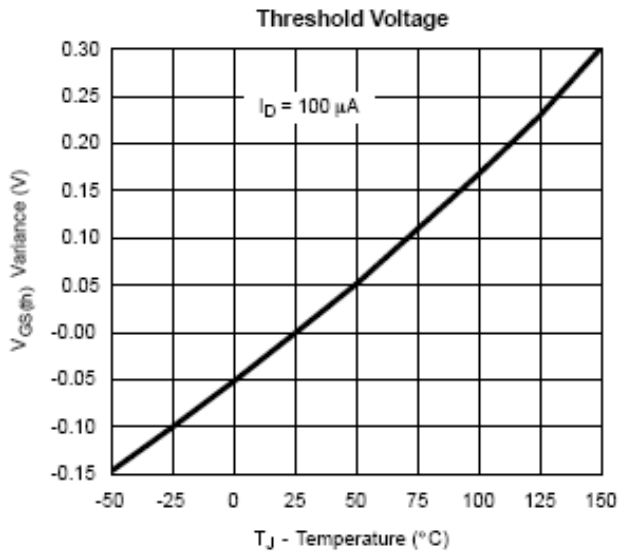




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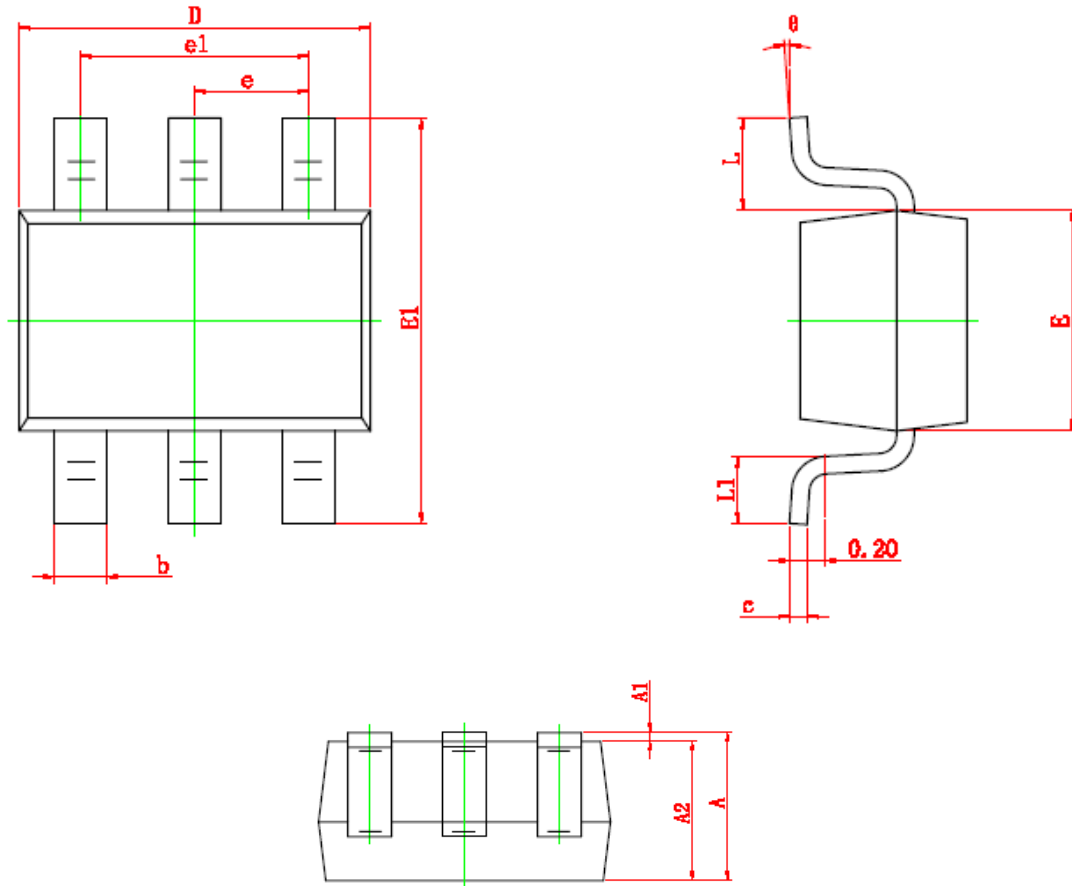




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SOT-363 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°



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