



SPP7413

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP7413 is the P-Channel logic enhancement mode power field effect transistors are produced using super high cell density , DMOS trench technology. The SPP7413 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low R_{DS(ON)} and fast switching speed.

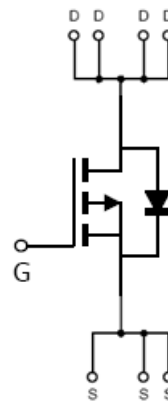
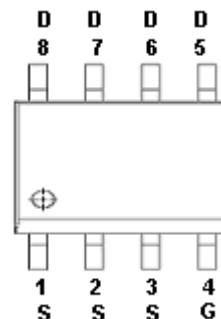
FEATURES

- -100V/-3A,R_{DS(ON)}=264mΩ@V_{GS}=-10V
- -100V/-2A,R_{DS(ON)}=324mΩ@V_{GS}=-4.5V
- High density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

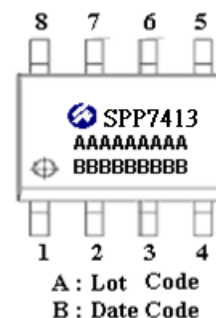
APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch
- Power Tool
- Motor Control

PIN CONFIGURATION(SOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP7413S8RGB	SOP-8	SPP7413

※ SPP7413S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-3.0
		TA=70°C	-2.0
Pulsed Drain Current	I _{DM}	-20	A
Power Dissipation	P _D	2.8	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	62.5	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	-1.0		-2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-80V, V_{GS}=0V$ $T_J=25^\circ C$			-1.0	uA
		$V_{DS}=-80V, V_{GS}=0V$ $T_J=55^\circ C$			-100	
Continuous-Source Current	I_S	$V_D=V_G=0V$, Force Cuent			-9	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3A$		223	264	mΩ
		$V_{GS}=-4.5V, I_D=-2A$		253	324	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=V_{GS}=0V$			-3.0	A
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-1A$		2.9		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-50V,$ $V_{GS}=-10V, I_D=-1A$		20		nC
Gate-Source Charge	Q_{gs}			4.1		
Gate-Drain Charge	Q_{gd}			5.1		
Input Capacitance	C_{iss}	$V_{DS}=-30, V_{GS}=0V$ $f=1MHz$		1029		pF
Output Capacitance	C_{oss}			68		
Reverse Transfer Capacitance	C_{rss}			39		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-30V,$ $I_D=-1.5A,$ $V_{GEN}=-10V, R_G=6\Omega$		10		nS
	t_r			9.5		
Turn-Off Time	$t_{d(off)}$			54		
	t_f			29		



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TYPICAL CHARACTERISTICS

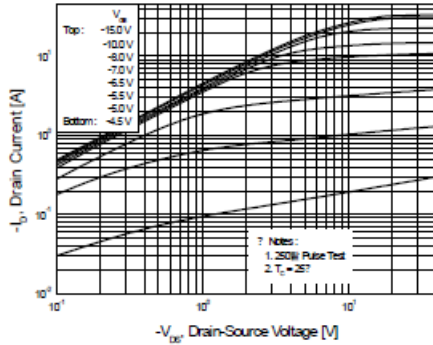


Figure 1. On-Region Characteristics

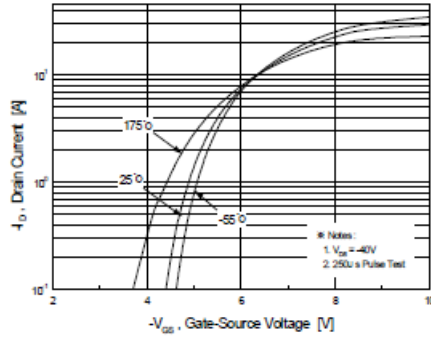


Figure 2. Transfer Characteristics

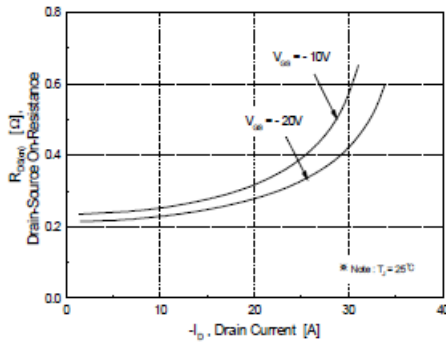


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

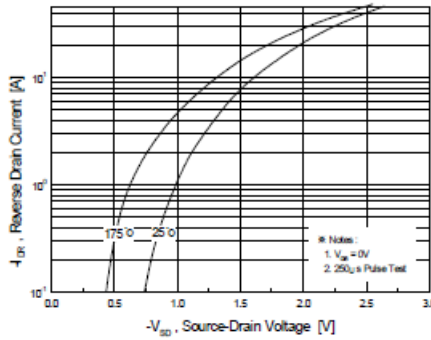


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

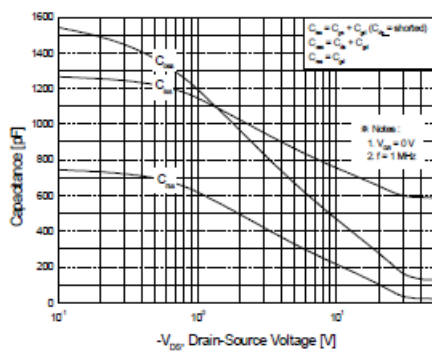


Figure 5. Capacitance Characteristics

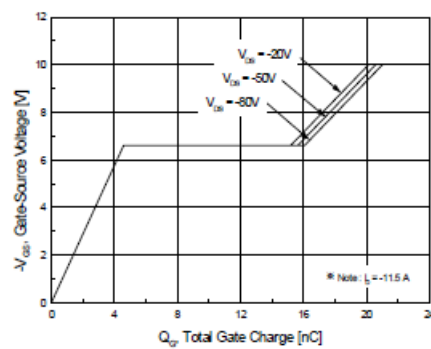


Figure 6. Gate Charge Characteristics



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TYPICAL CHARACTERISTICS

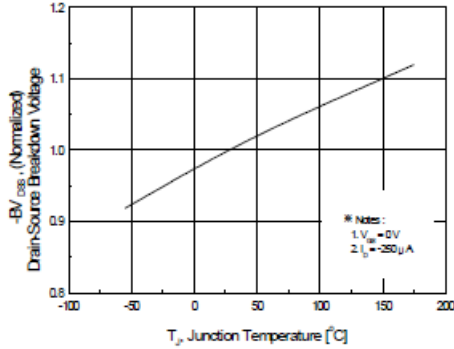


Figure 7. Breakdown Voltage Variation vs. Temperature

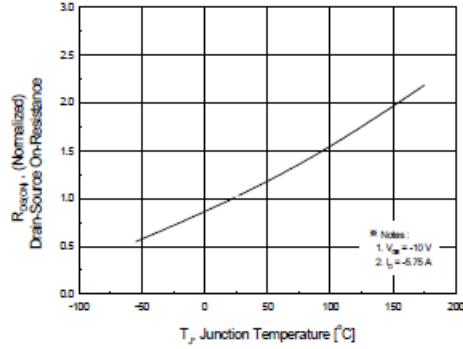


Figure 8. On-Resistance Variation vs. Temperature

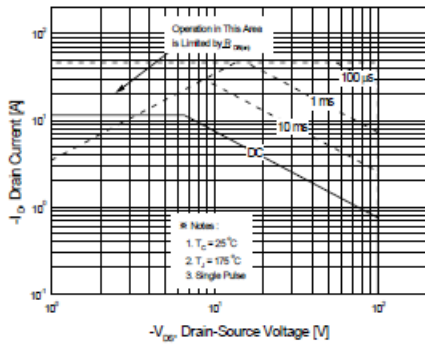


Figure 9. Maximum Safe Operating Area

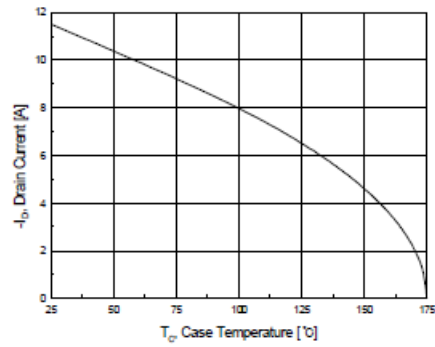


Figure 10. Maximum Drain Current vs. Case Temperature

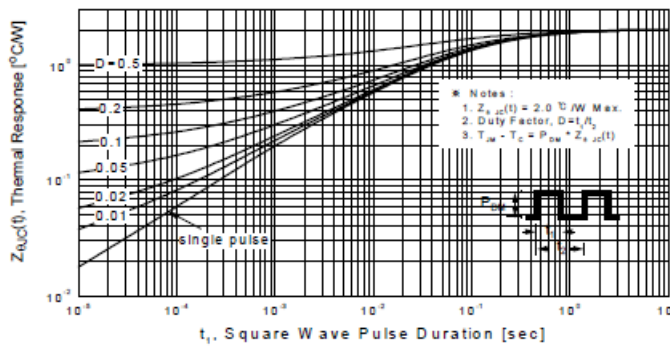


Figure 11. Transient Thermal Response Curve



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