



SPP8625

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8625 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

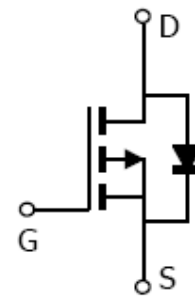
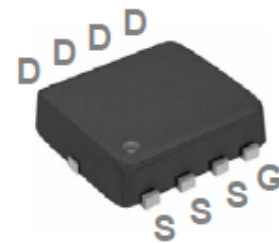
FEATURES

- -12V/-9.0A, $R_{DS(ON)}=19.5m\Omega@V_{GS}=-4.5V$
- -12V/-8.5A, $R_{DS(ON)}=25m\Omega@V_{GS}=-2.5V$
- Super high density cell design for extremely Low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L package design

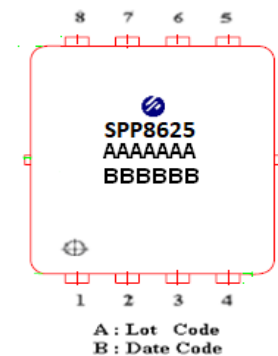
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (PPAK3x3-8L)



PART MARKING





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PPAK3x3-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8625DN8RGB	PPAK3x3-8L	SPP8625

※ SPP8625DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-12	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current (T _J =150°C)	I _D	TA=25°C	-9.0	A
		TA=70°C	-7.2	
Pulsed Drain Current	I _{DM}	-42	A	
Power Dissipation	P _D	TA=25°C	2	W
		TA=70°C	1.3	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	62	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-12			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35	-0.5	-0.9	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 8.0V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-12V, V_{GS}=0V$			-1	uA
		$V_{DS}=-12V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-4.5V$	-60			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-9.0A$		15.5	19.5	mΩ
		$V_{GS}=-2.5V, I_D=-8.5A$		20	25	
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-9.0A$		45		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$		-0.53	-1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-6V, V_{GS}=-4.5V$ $I_D=-9.0A$		19	23	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			5.3		
Input Capacitance	C_{iss}	$V_{DS}=-6V, V_{GS}=0V$ $f=1MHz$		1740	2100	pF
Output Capacitance	C_{oss}			334		
Reverse Transfer Capacitance	C_{rss}			200		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-6V, R_L=0.67\Omega$ $V_{GEN}=-4.5V, R_G=3\Omega$		240		nS
	t_r			580		
Turn-Off Time	$t_{d(off)}$				7.0	uS
	t_f				4.2	



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TYPICAL CHARACTERISTICS

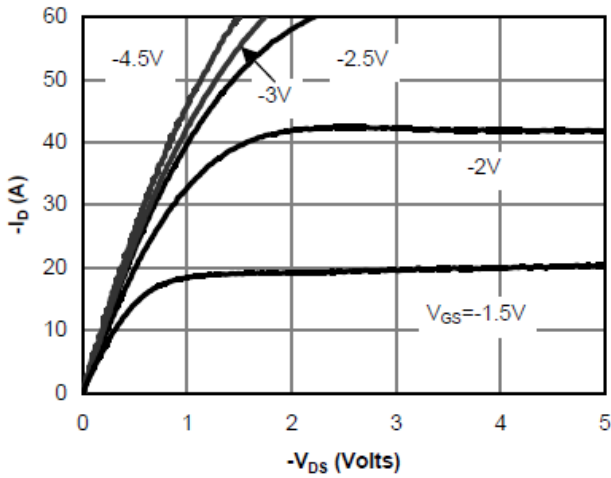


Figure 1: On-Region Characteristics(Note E)

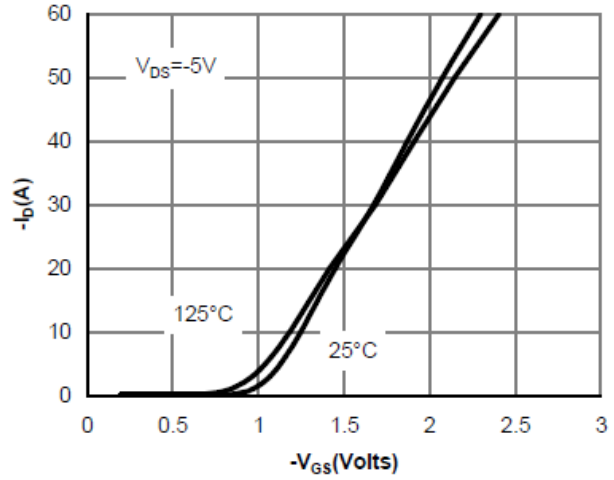


Figure 2: Transfer Characteristics(Note E)

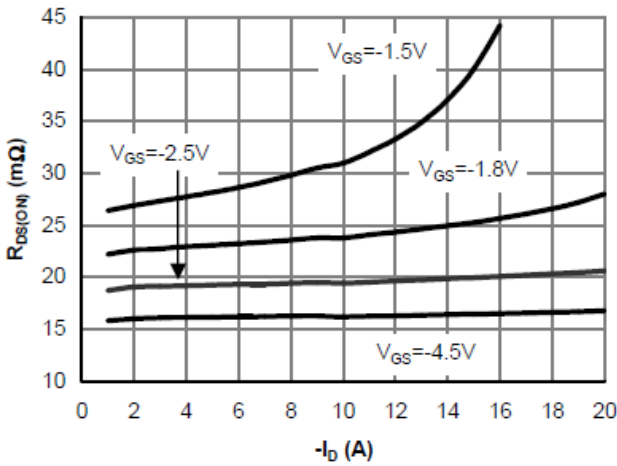


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

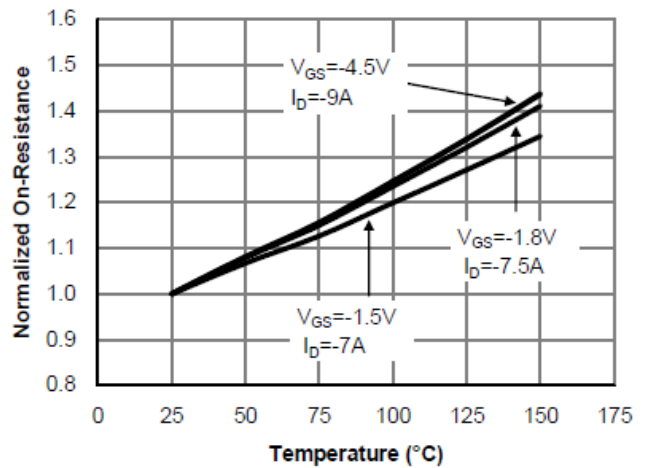


Figure 4: On-Resistance vs. Junction Temperature(Note E)

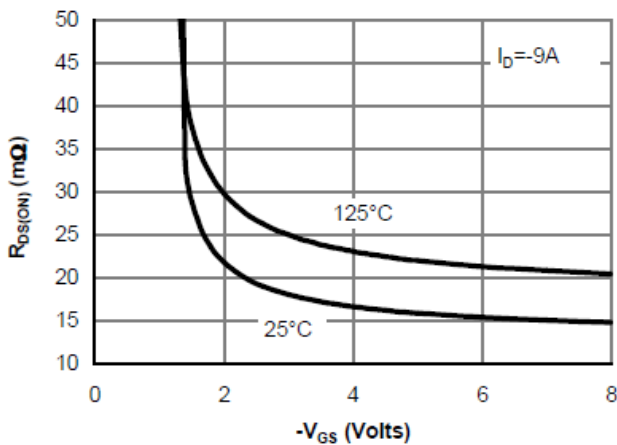


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

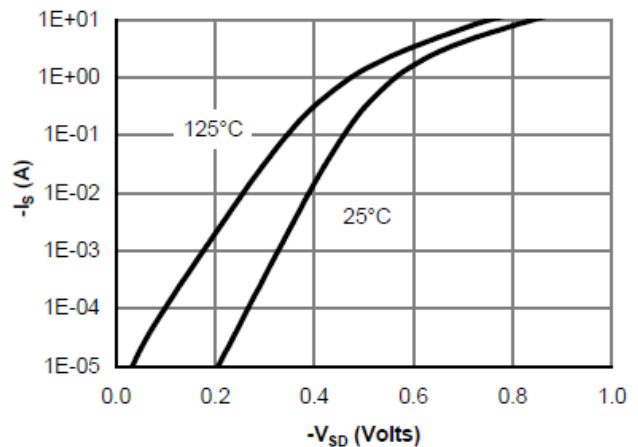


Figure 6: Body-Diode Characteristics(Note E)



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TYPICAL CHARACTERISTICS

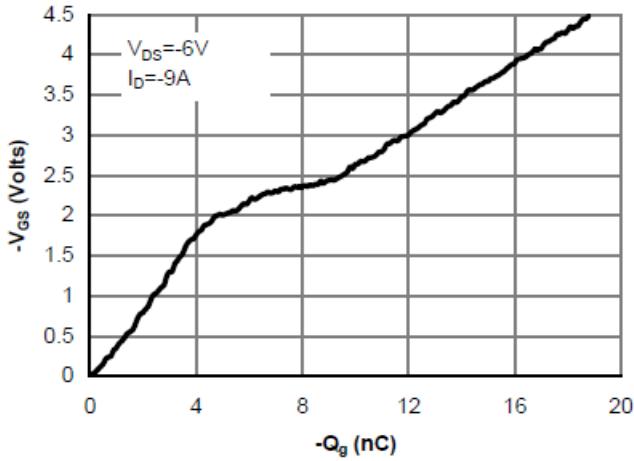


Figure 7: Gate-Charge Characteristics

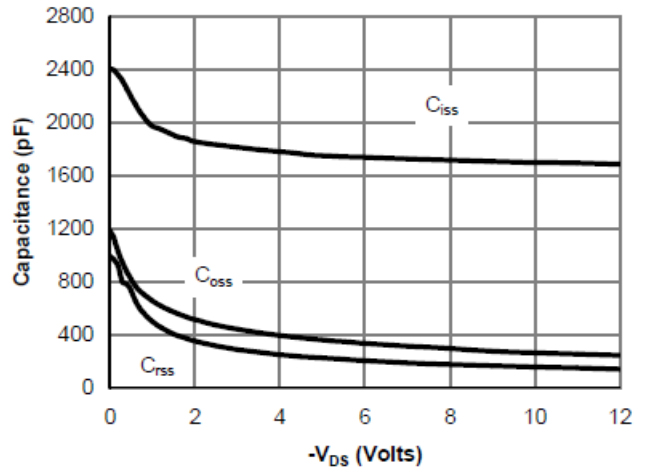


Figure 8: Capacitance Characteristics

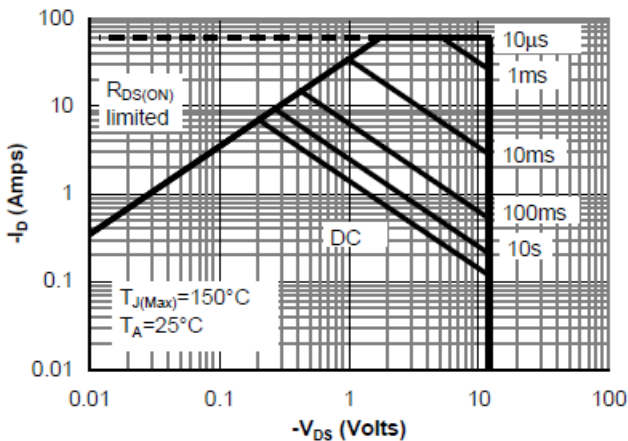


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

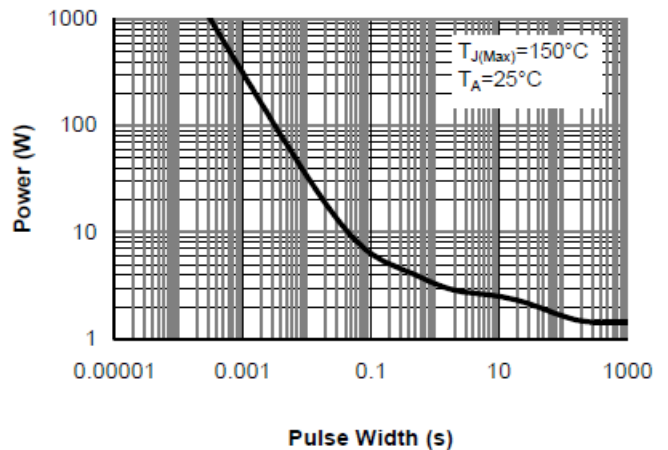


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

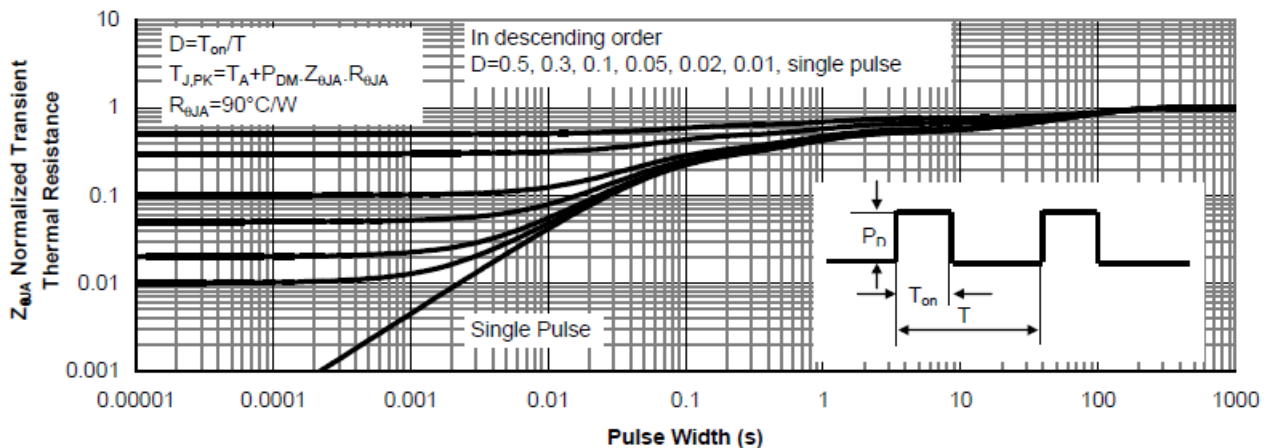


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



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