



SPP8803

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8803 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

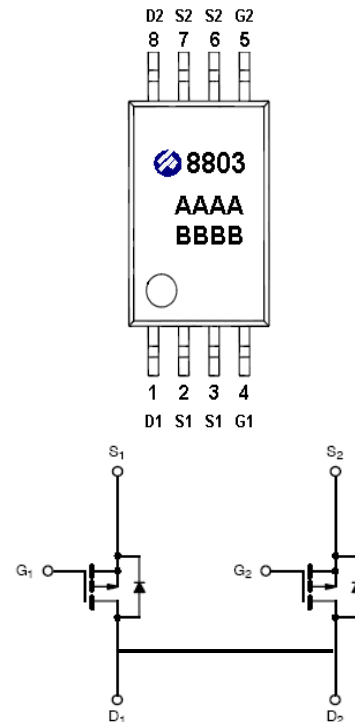
FEATURES

- ◆ -20V/-7.0A, $R_{DS(ON)} = 20m\Omega @ V_{GS} = -4.5V$
- ◆ -20V/-6.0 A, $R_{DS(ON)} = 25m\Omega @ V_{GS} = -2.5V$
- ◆ -20V/-5.0 A, $R_{DS(ON)} = 35m\Omega @ V_{GS} = -1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TSSOP-8P package design

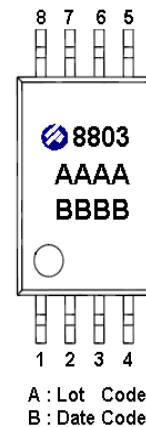
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(TSSOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	D1	Drain
2	S1	Source
3	S1	Source
4	G1	Gate
5	G2	Gate
6	S2	Source
7	S2	Source
8	D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8803TS8RGB	TSSOP- 8P	8803

※ SPP8803TS8RGB : 13" Tape Reel ; Pb – Free; Halogen -Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-7.0	A
		TA=70°C	-5.8	
Pulsed Drain Current	I _{DM}	-30	A	
Continuous Source Current(Diode Conduction)	I _S	-2.3	A	
Power Dissipation	P _D	TA=25°C	1.5	W
		TA=70°C	0.9	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W	



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ELECTRICAL CHARACTERISTICS

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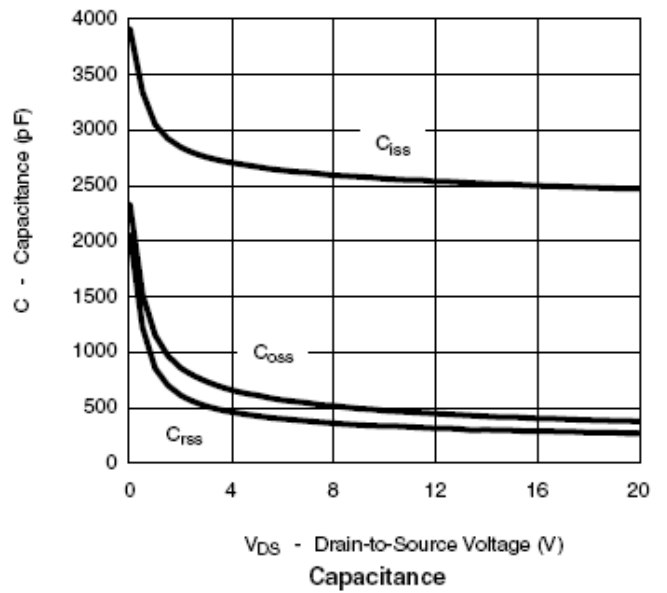
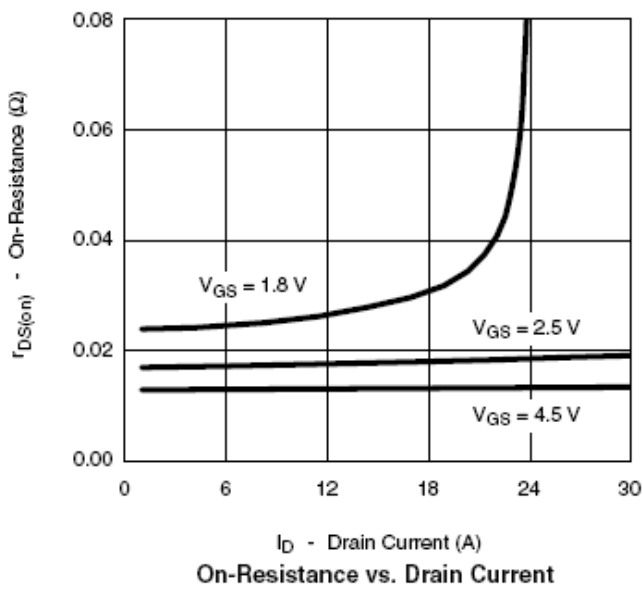
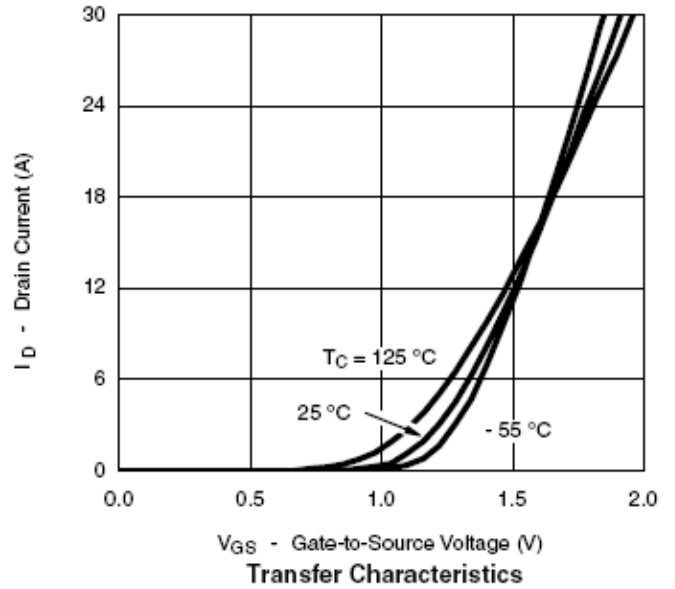
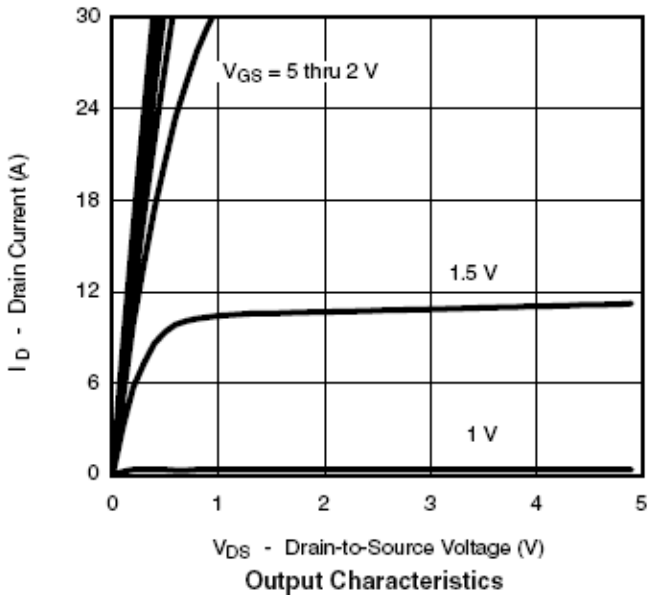
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.9	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$			-1	uA
		$V_{DS}=-20V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-4.5V$	-20			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-7.0A$		0.016	0.020	Ω
		$V_{GS}=-2.5V, I_D=-6.0A$		0.020	0.025	
		$V_{GS}=-1.8V, I_D=-5.0A$		0.028	0.035	
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-10.0A$		36		S
Diode Forward Voltage	V_{SD}	$I_S=-2.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V, V_{GS}=-5.0V$ $I_D=-10.0A$		30	45	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			8.0		
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V$ $f=1MHz$		2670		pF
Output Capacitance	C_{oss}			520		
Reverse Transfer Capacitance	C_{rss}			480		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6\Omega$		25	40	ns
	t_r			45	70	
Turn-Off Time	$t_{d(off)}$			145	240	
	t_f			70	115	



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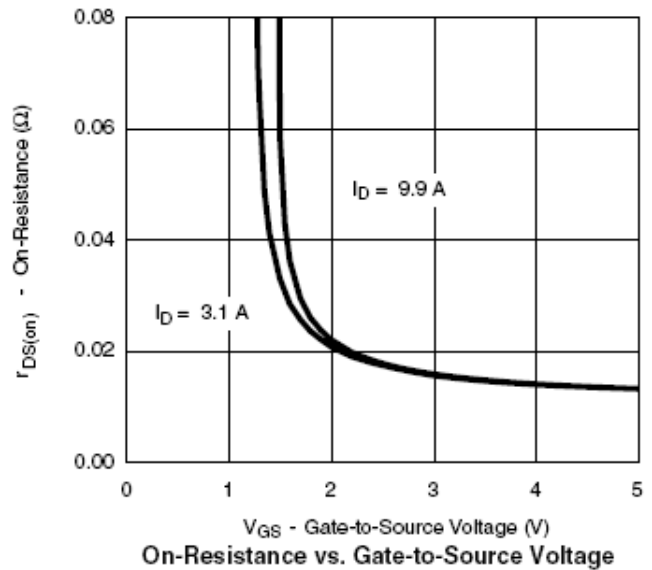
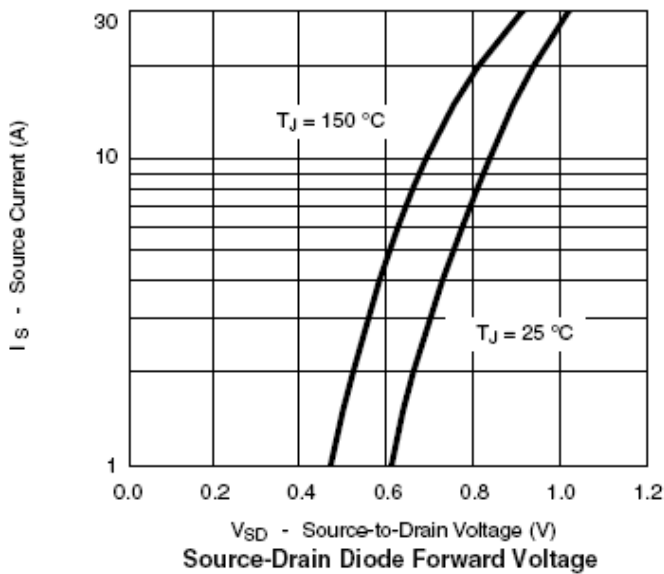
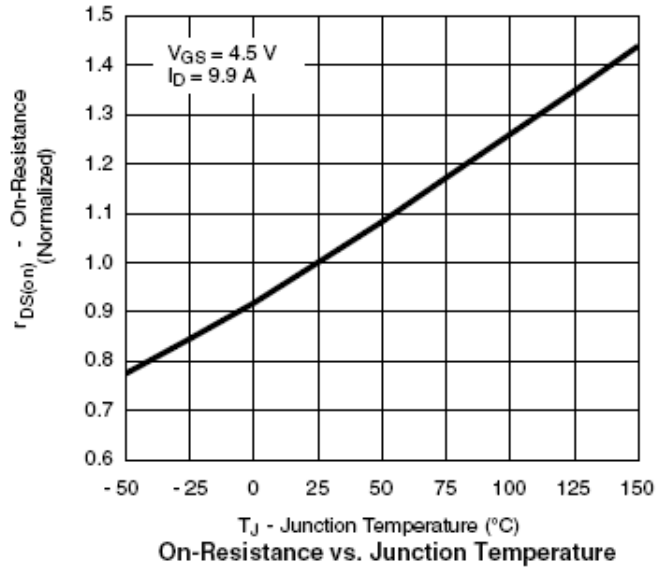
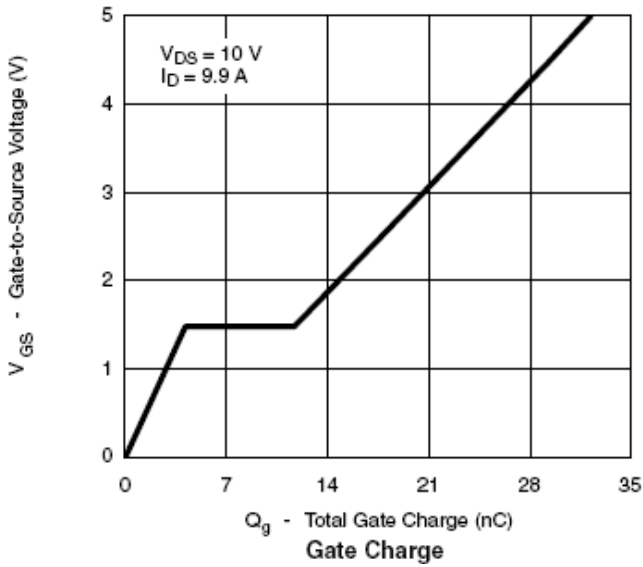
TYPICAL CHARACTERISTICS





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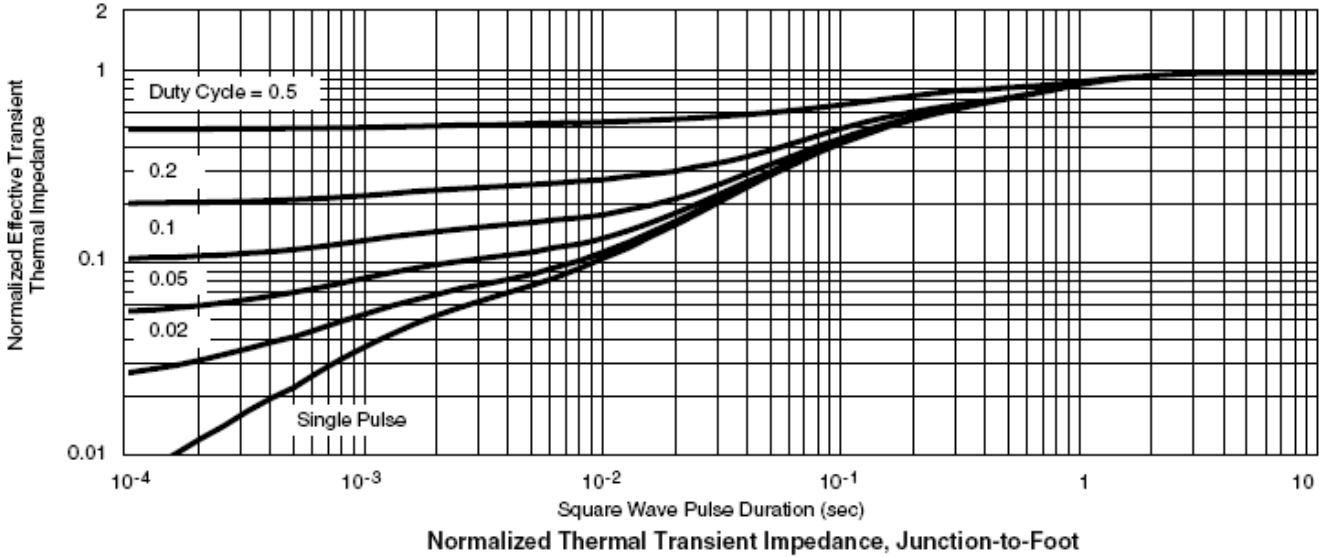
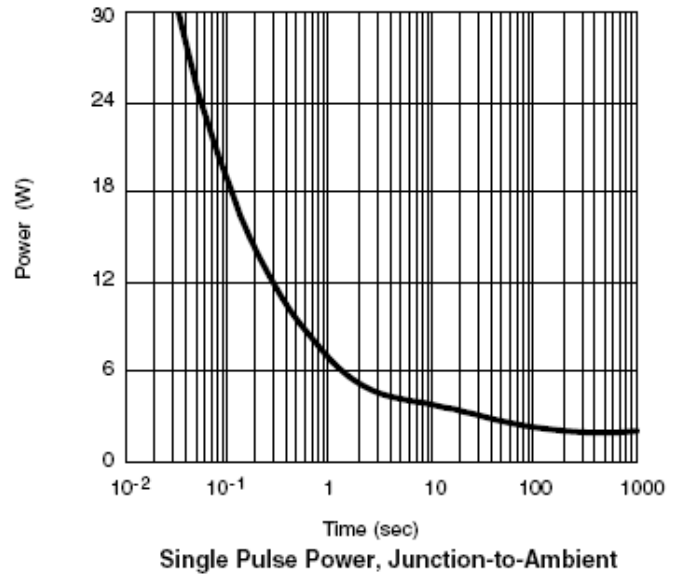
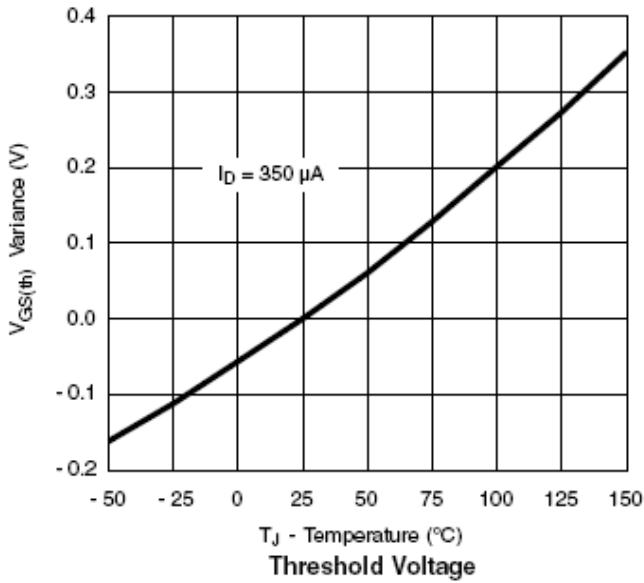
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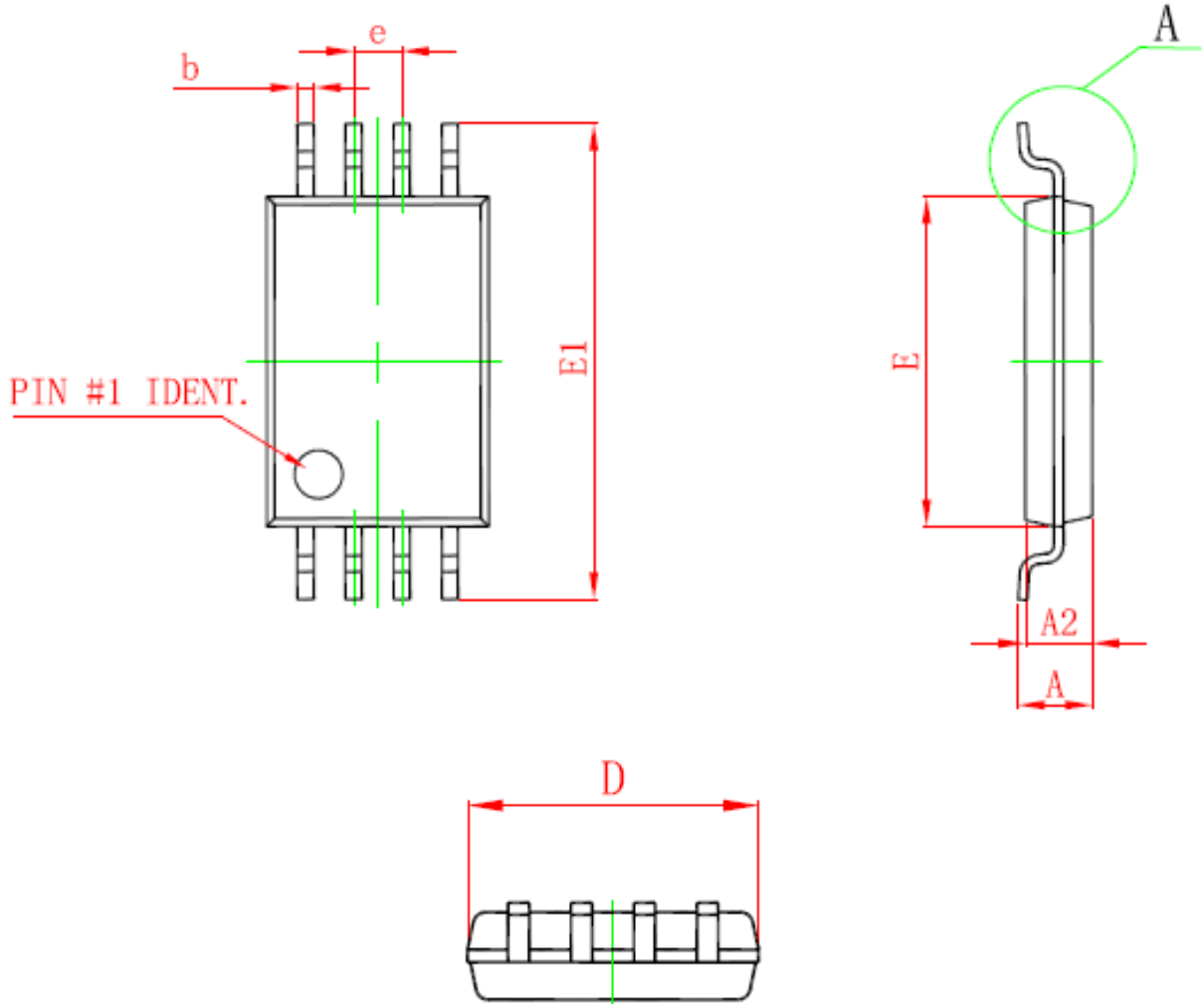




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TSSOP- 8P PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°



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