



SPP8805

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8805 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

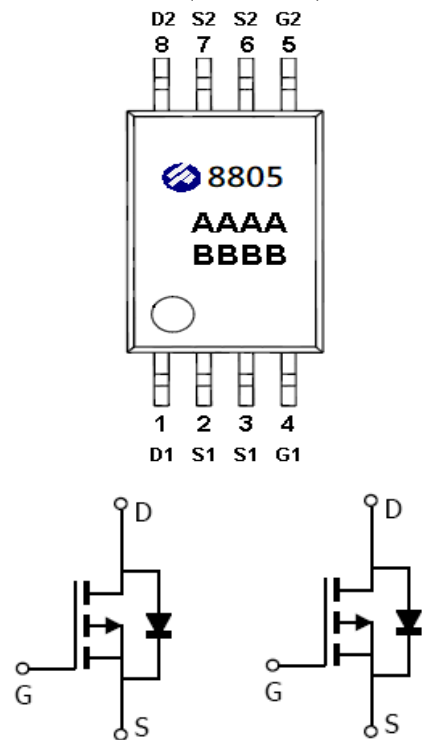
FEATURES

- ◆ -20V/-7.2A, $R_{DS(ON)}=40m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-5.2A, $R_{DS(ON)}=52m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-3.6A, $R_{DS(ON)}=70m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely Low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TSSOP-8 package design

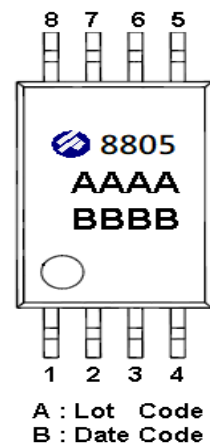
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (TSSOP-8)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	D1	Drain
2	S1	Source
3	S1	Source
4	G1	Gate
5	G2	Gate
6	S2	Source
7	S2	Source
8	D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8805TS8RGB	TSSOP-8	8805

※ SPP8805TS8RGB : 13" Tape Reel ; Pb – Free; Halogen -Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-20	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	-7.6
		T _A =70°C	-5.4
Pulsed Drain Current	I _{DM}	-30	A
Continuous Source Current(Diode Conduction)	I _S	-2.3	A
Power Dissipation	P _D	T _A =25°C	2.8
		T _A =70°C	1.8
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	70	°C/W



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ELECTRICAL CHARACTERISTICS

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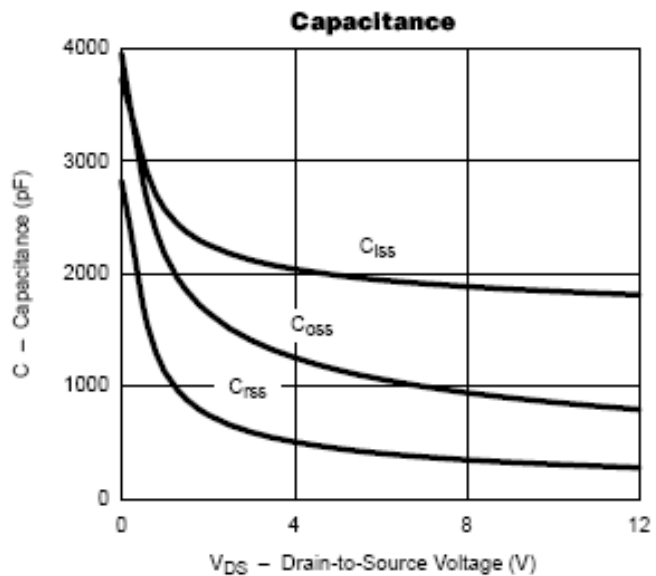
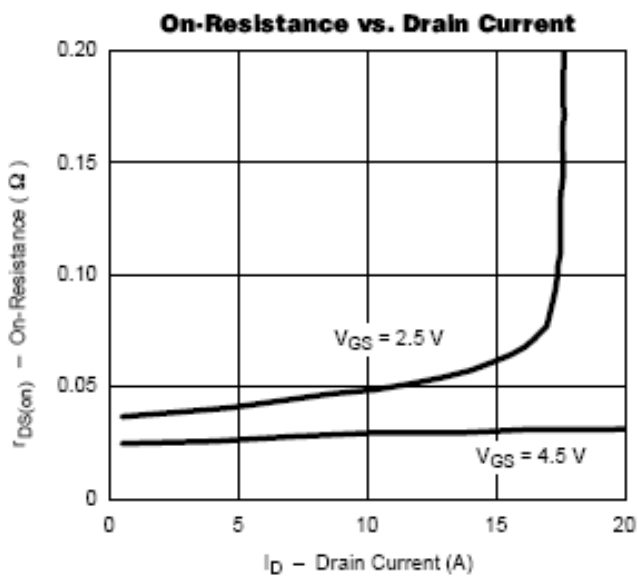
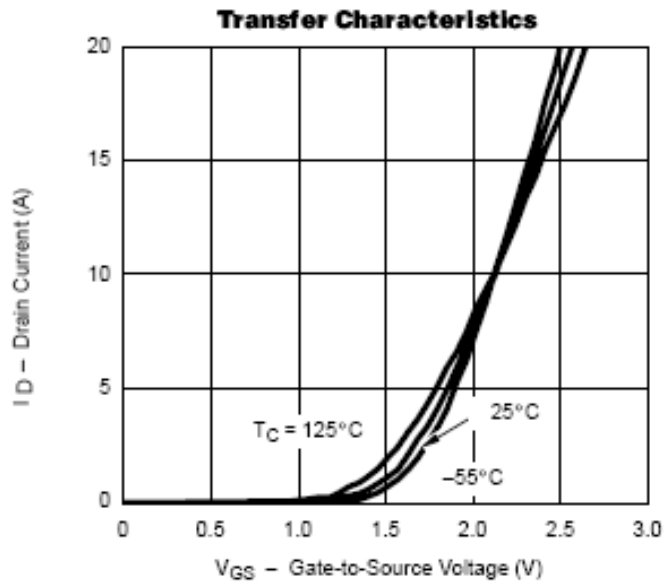
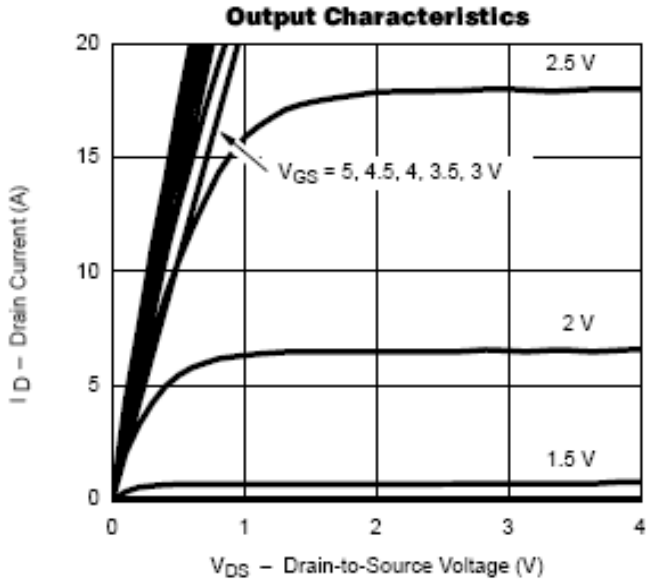
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.35		-0.9	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$			-1	uA
		$V_{DS}=-16V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-4.5V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-7.2A$		0.030	0.040	Ω
		$V_{GS}=-2.5V, I_D=-5.2A$		0.040	0.052	
		$V_{GS}=-1.8V, I_D=-3.6A$		0.055	0.070	
Forward Transconductance	g_{fs}	$V_{DS}=-5.0V, I_D=-6.2A$		14		S
Diode Forward Voltage	V_{SD}	$I_S=-2.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-10V, V_{GS}=-4.5V$ $I_D=-6.4A$		20	25	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			8.0		
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V$ $f=1MHz$		700		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			120		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, R_L=6\Omega$ $I_D=-1.0A, V_{GEN}=-4.5V$ $R_G=6\Omega$		20	30	nS
	t_r			40	65	
Turn-Off Time	$t_{d(off)}$			90	120	
	t_f			70	90	



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TYPICAL CHARACTERISTICS

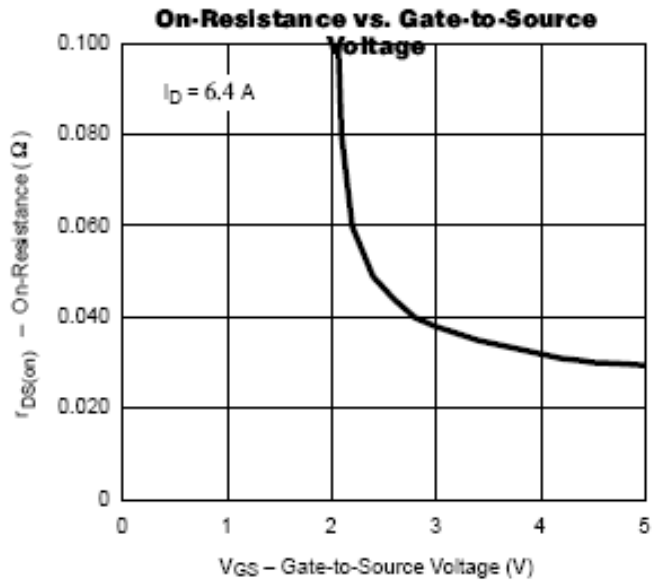
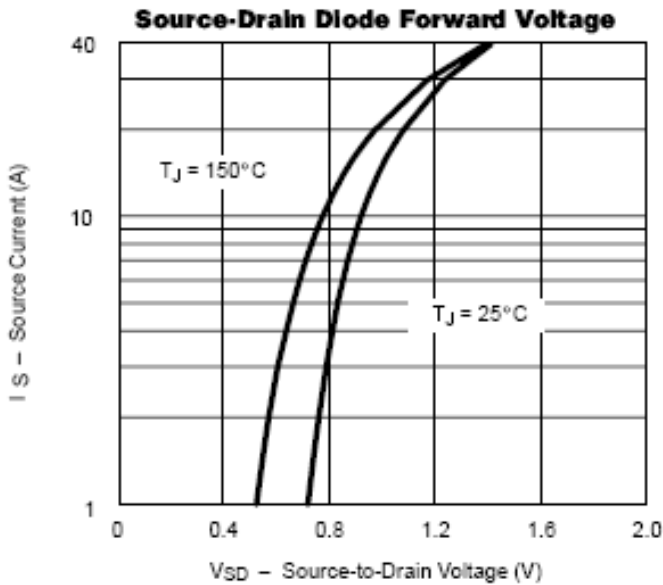
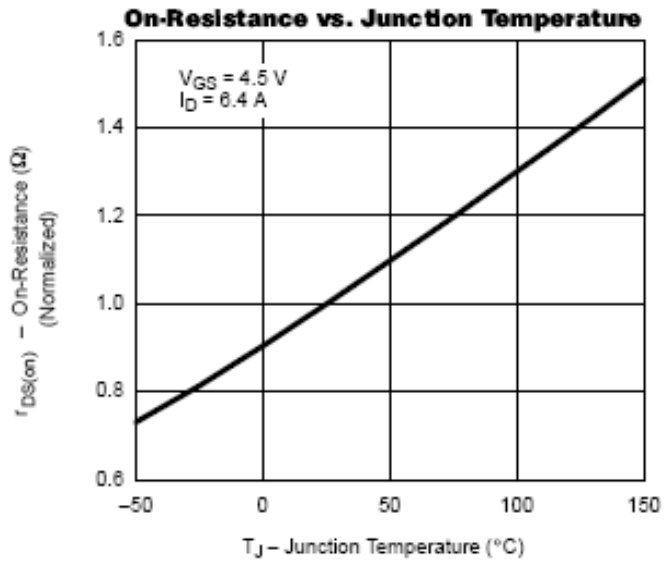
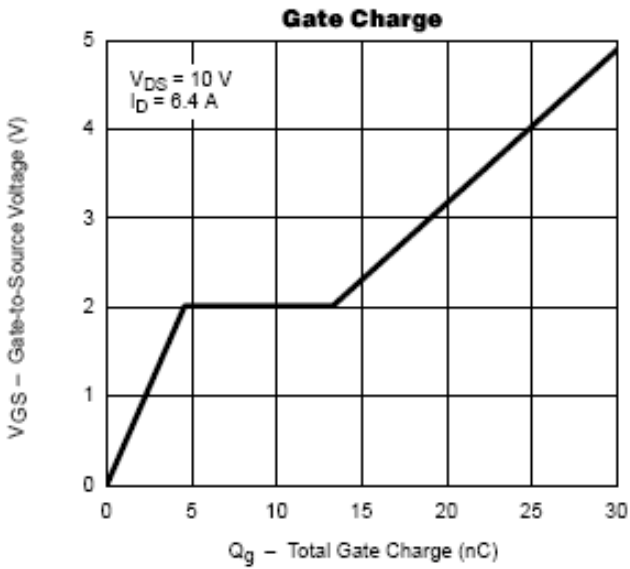




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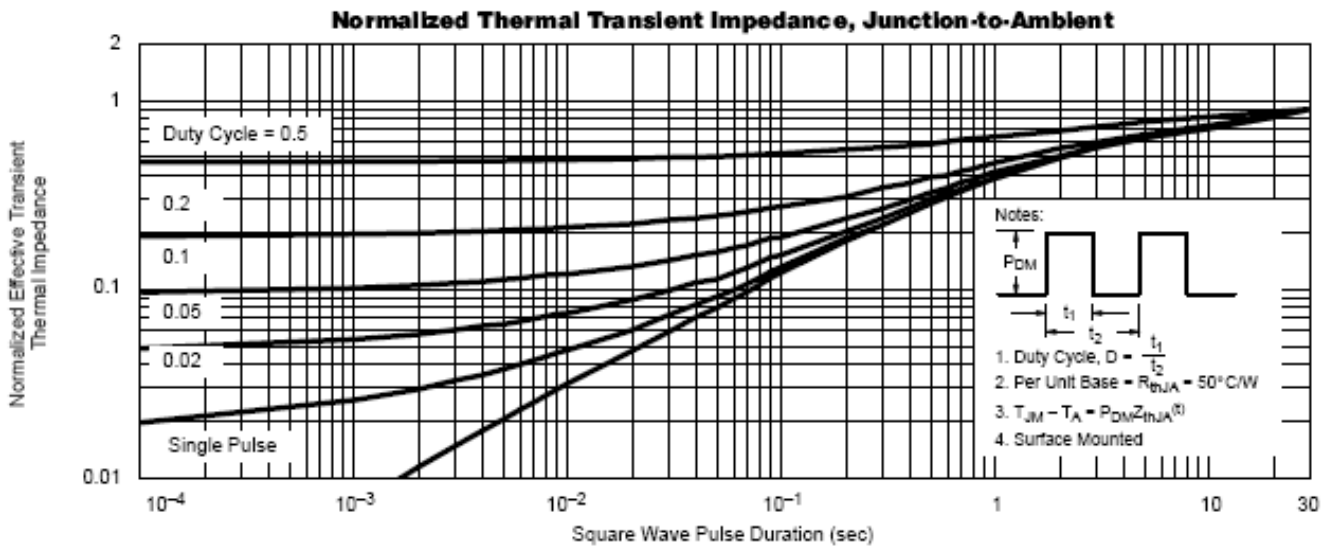
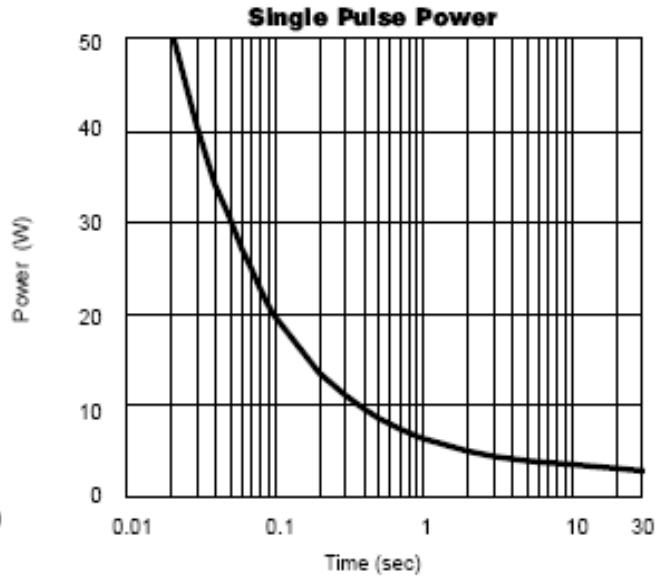
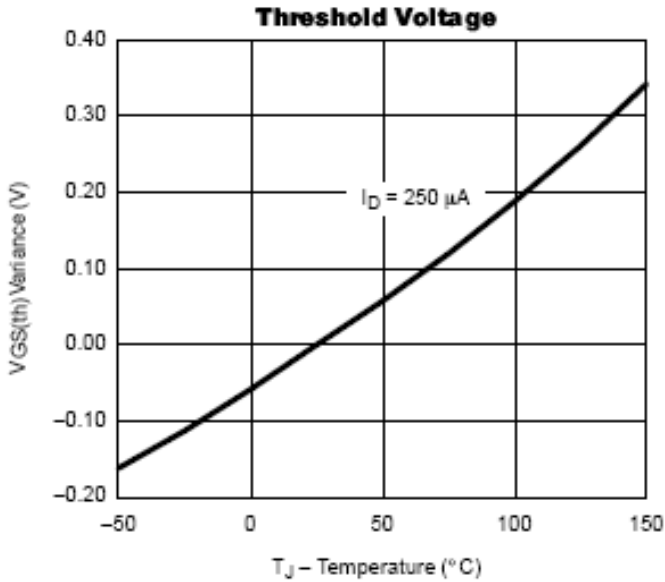




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