



SPP8813

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8813 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP8813 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

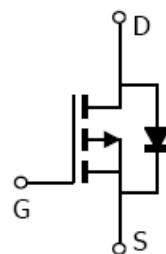
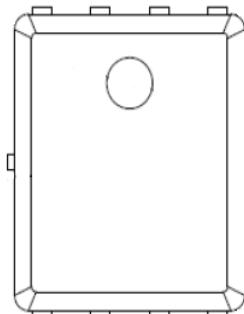
FEATURES

- ◆ -80V/-4A, $R_{DS(ON)}=85\text{m}\Omega$ @ $V_{GS}=-10\text{V}$
- ◆ -80V/-3A, $R_{DS(ON)}=100\text{m}\Omega$ @ $V_{GS}=-4.5\text{V}$
- ◆ High density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

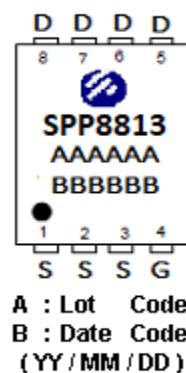
APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION (PPAK5x6-8L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8813DN8RGB	PPAK5x6-8L	SPP8813

※ SPP8813DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-80	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current	T _c =25°C	-13	A
Continuous Drain Current		-11	
Pulsed Drain Current	I _{DM}	-20	A
Avalanche Energy, Single Pulse (L=0.1mH , T _c =25°C)	E _{AS}	11.25	mJ
Power Dissipation @ T _c =25°C	P _D	52	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	1.9	°C/W



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ELECTRICAL CHARACTERISTICS

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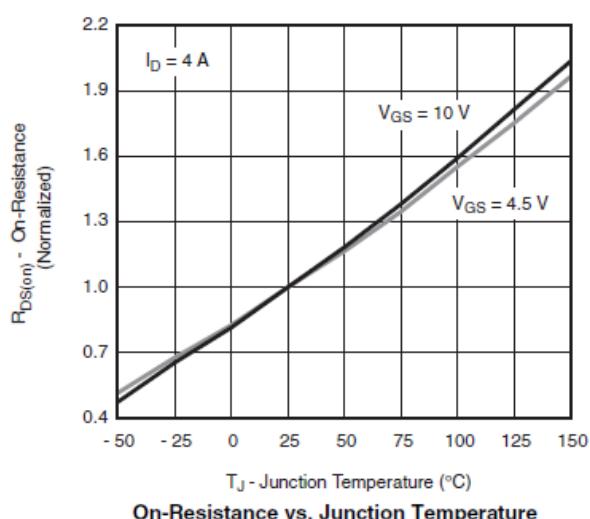
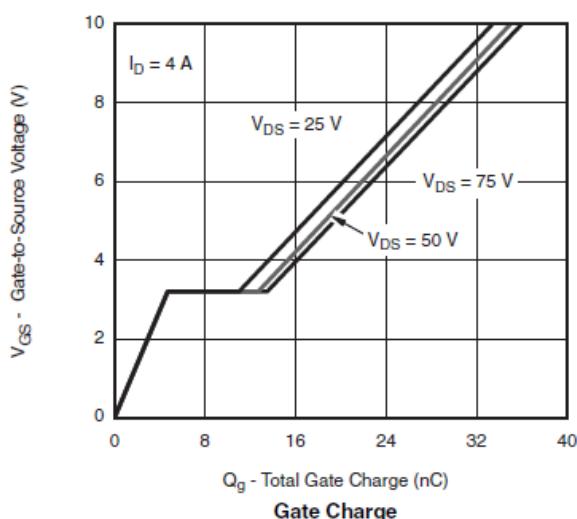
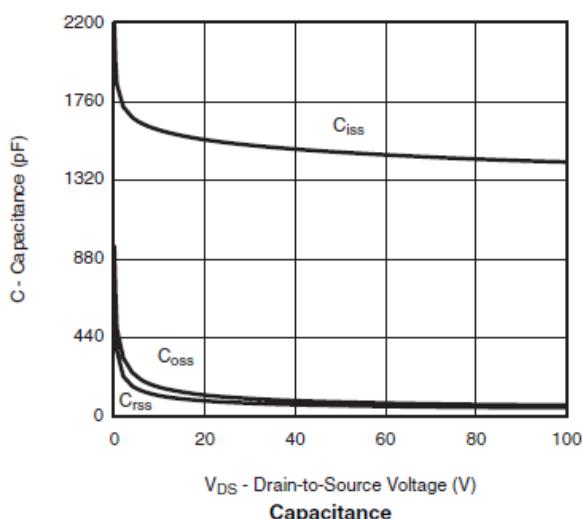
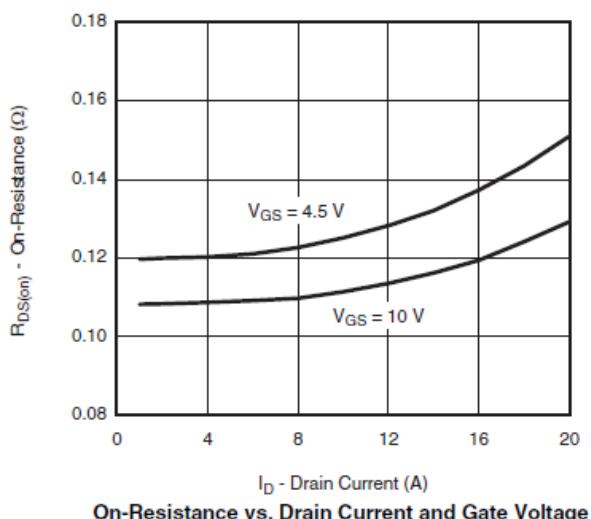
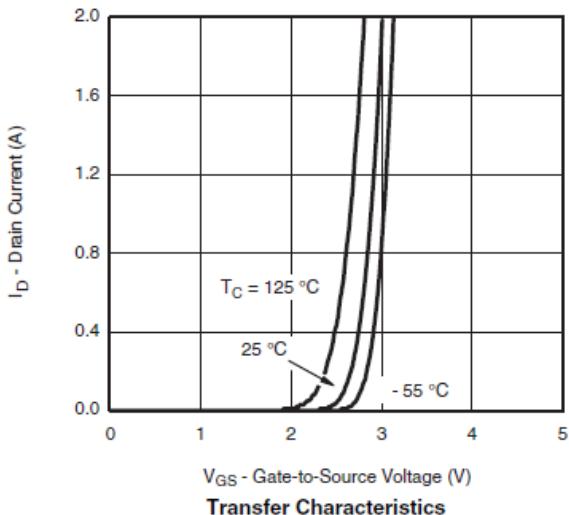
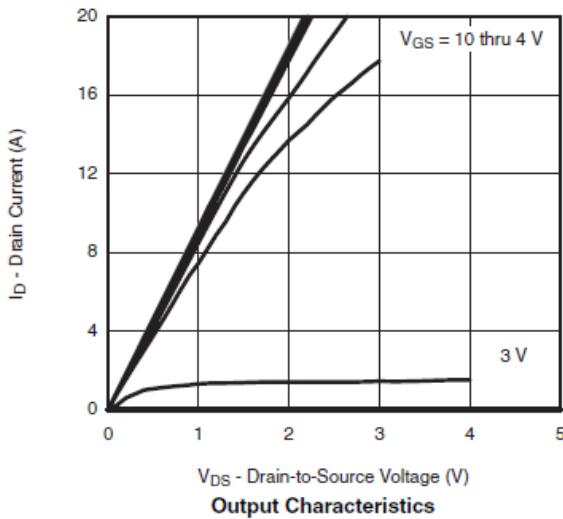
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-80			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1		-3	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-64V, V _{GS} =0V			-1	
		V _{DS} =-64V, V _{GS} =0V T _J =55°C			-10	uA
On-State Drain Current	I _{D(on)}	V _{DS} ≥-5V, V _{GS} =-10V	-10			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =-10V, I _D =-4.0A		75	85	
		V _{GS} = -4.5V, I _D =-3.0A		85	100	mΩ
Forward Transconductance	g _{fs}	V _{DS} =-15V, I _D =-4A		25		S
Diode Forward Voltage	V _{SD}	I _S =-3A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _{g(10V)}	V _{DS} =-50V , V _{GS} =-10V I _D =-4A		35	55	
Total Gate Charge	Q _{g(4.5V)}	V _{DS} =-50V , V _{GS} =-4.5V I _D =-4A		16.5	25	
Gate-Source Charge	Q _{gs}			4.7		
Gate-Drain Charge	Q _{gd}			8		
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V f=1MHz		1480		
Output Capacitance	C _{oss}			80		pF
Reverse Transfer Capacitance	C _{rss}			60		
Turn-On Time	t _{d(on)}	V _{DD} =-50V, I _D =-4A, V _{GEN} =-10V R _G =1Ω		11	18	
	t _r			13	20	
Turn-Off Time	t _{d(off)}			42	65	
	t _f			10	15	nS



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TYPICAL CHARACTERISTICS

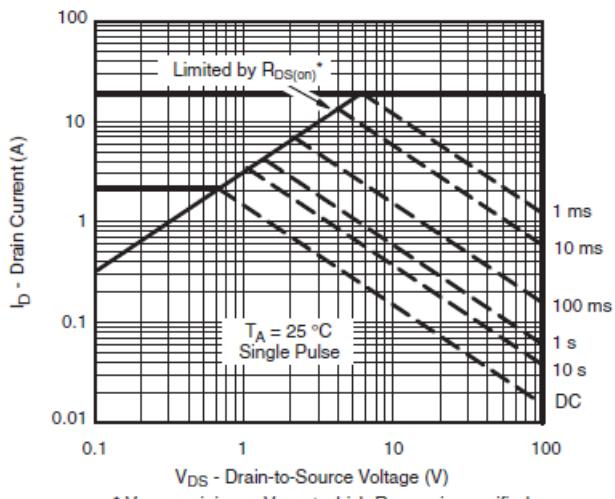
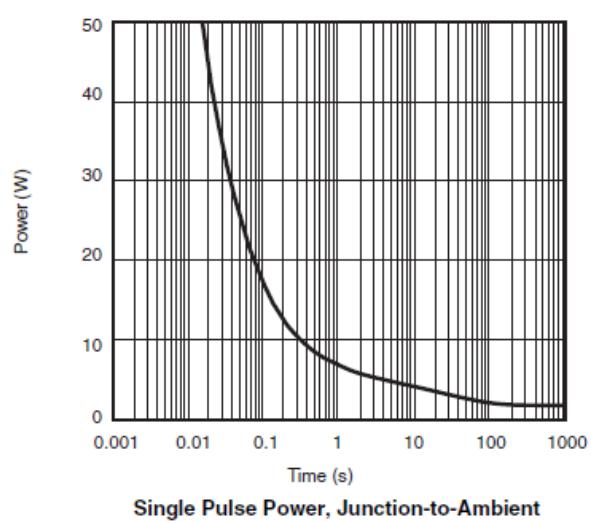
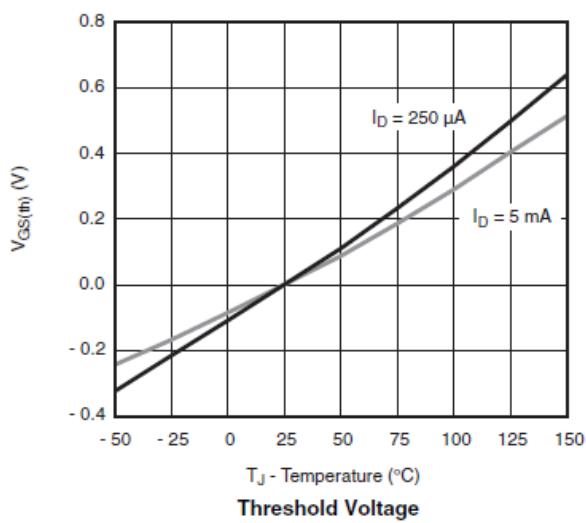
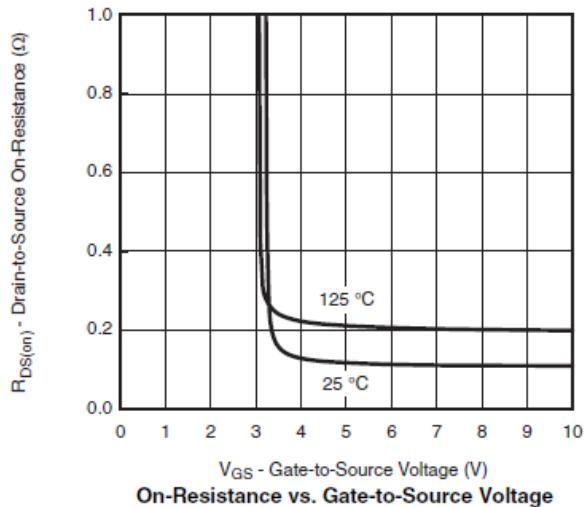
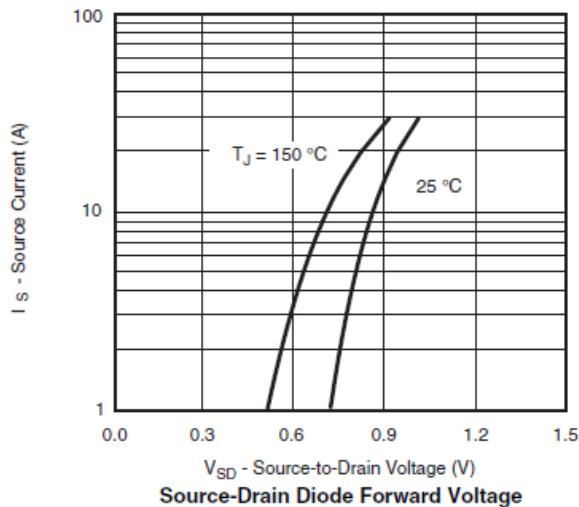




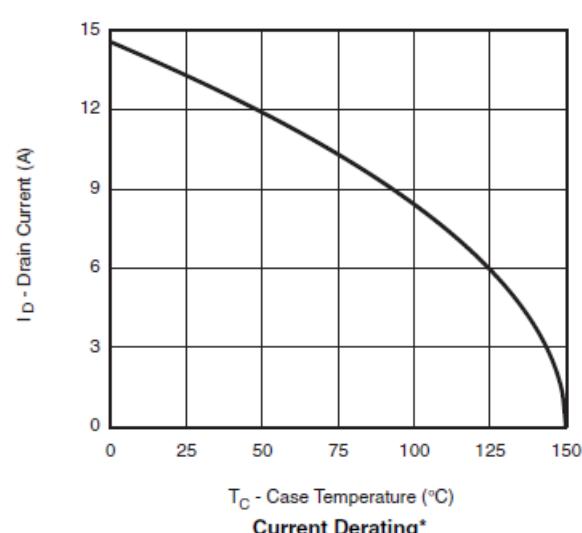
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TYPICAL CHARACTERISTICS



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

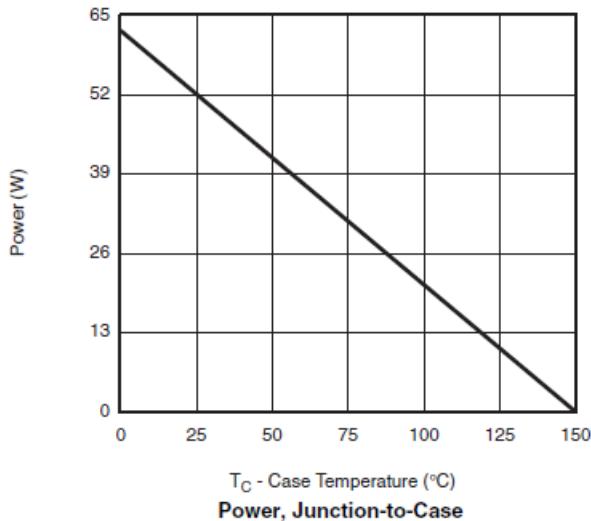




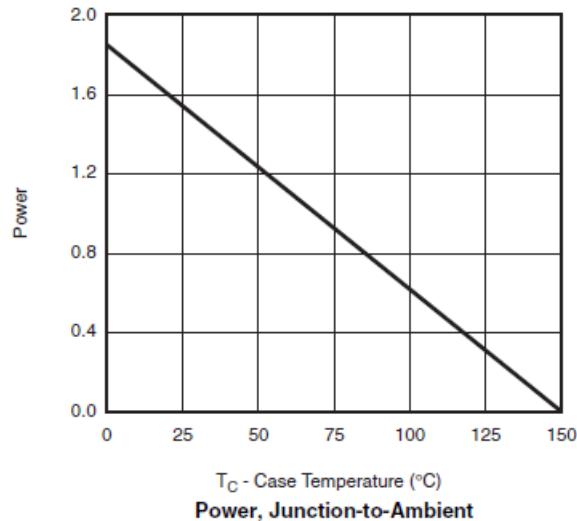
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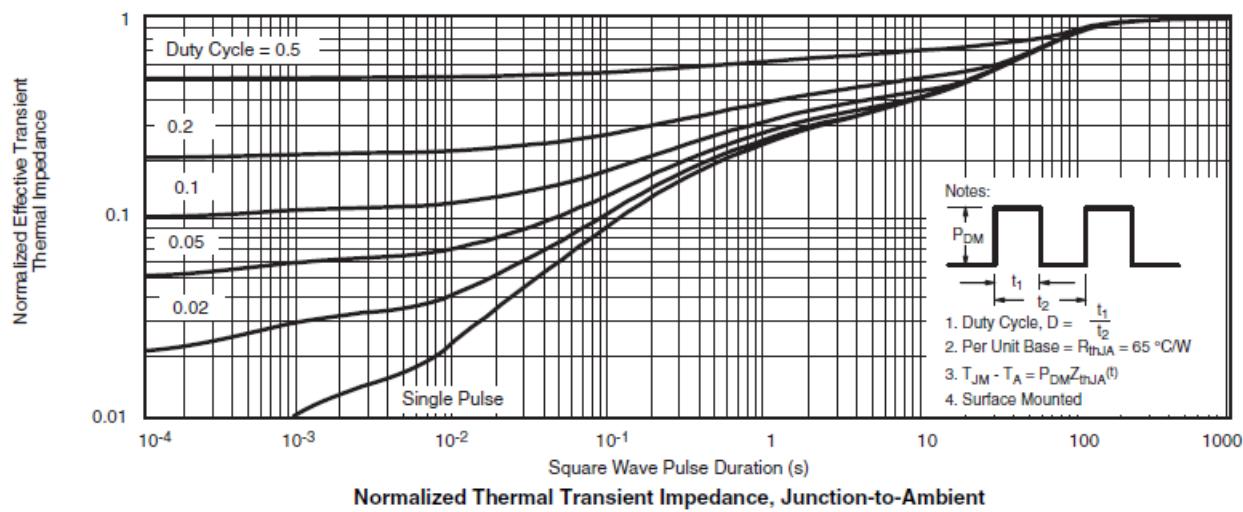
TYPICAL CHARACTERISTICS



T_C - Case Temperature (°C)
Power, Junction-to-Case



T_C - Case Temperature (°C)
Power, Junction-to-Ambient





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