SPP8845
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8845 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP8845 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

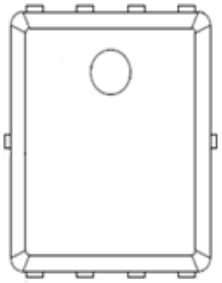
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

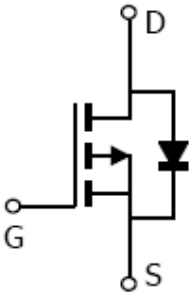
FEATURES

- -40V/-25A,$R_{DS(ON)}$=5.8mΩ@V_{GS}=-10V
- -40V/-12A,$R_{DS(ON)}$=8.5mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

PIN CONFIGURATION

PPAK5x6-8L





PART MARKING

A : Lot Code
B : Date Code
(YY / MM / DD)

SPP8845
P-Channel Enhancement Mode MOSFET

PPAK5X6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8845DN8RGB	PPAK5x6-8L	SPP8845

※ SPP8845DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	-85	A
	T_A=100℃		-54	
Pulsed Drain Current		I_{DM}	-340	A
Avalanche Current		I_{AS}	-70	A
Single Pulse Avalanche Energy (L=0.1mH , Tc=25℃)		E_{AS}	245	mJ
Power Dissipation	T_C=25℃	P_D	135	W
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	0.92	℃/W

SPP8845
P-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.2		-2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-32V,V_{GS}=0V			-1	uA
		V_{DS}=-32V,V_{GS}=0V,T_J=125℃			-10	
Gate Resistance	Rg	V_{DS}=0V,V_{GS}=0V,f=1MHz		4.2	6.3	Ω
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-25A		4.7	5.8	mΩ
		V_{GS}=-4.5V,I_D=-12A		6.4	8.5	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-3A		15		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V			-1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-32V,V_{GS}=-10V I_D=-10A		106	160	nC
Gate-Source Charge	Q_{gs}			13.1	20	
Gate-Drain Charge	Q_{gd}			24.9	38	
Input Capacitance	C_{iss}	V_{DS}=-25VV_{GS}=0V f=1MHz		5720	8580	pF
Output Capacitance	C_{oss}			527	790	
Reverse Transfer Capacitance	C_{rss}			352	528	
Turn-On Time	$t_{d(on)}$	V_{DD}=-32V, I_D=-1A,V_{GS}=-10V, R_G=6Ω		41.6	82	nS
	t_r			12.7	26	
Turn-Off Time	$t_{d(off)}$			308	600	
	t_f			70	140	

TYPICAL CHARACTERISTICS

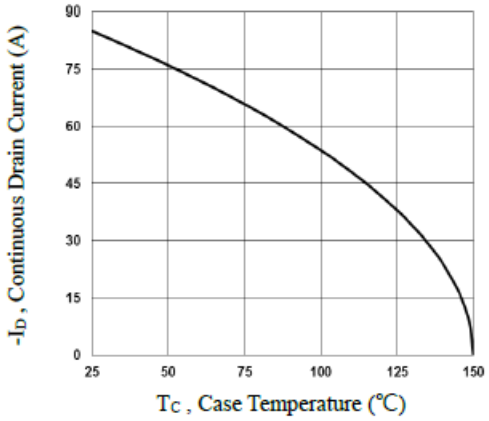


Fig.1 Continuous Drain Current vs. T_C

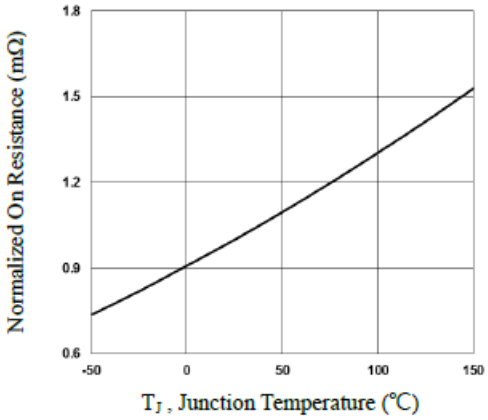


Fig.2 Normalized RDSON vs. T_J

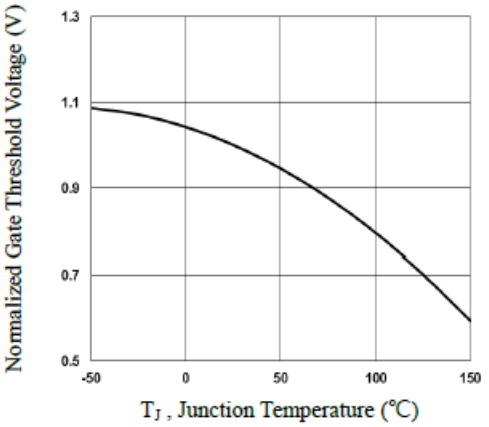


Fig.3 Normalized V_{th} vs. T_J

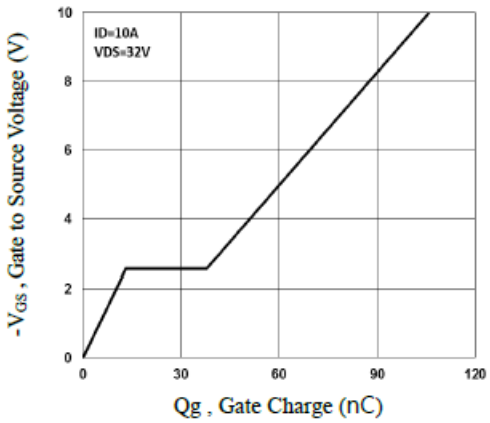


Fig.4 Gate Charge Waveform

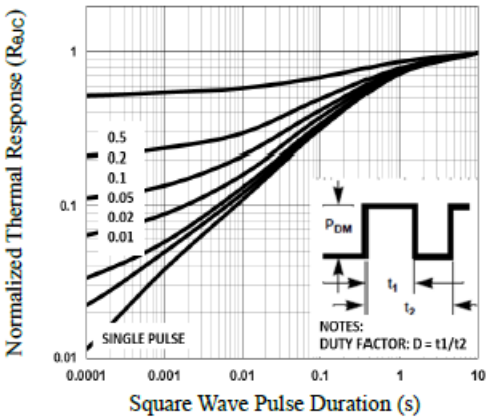


Fig.5 Normalized Transient Impedance

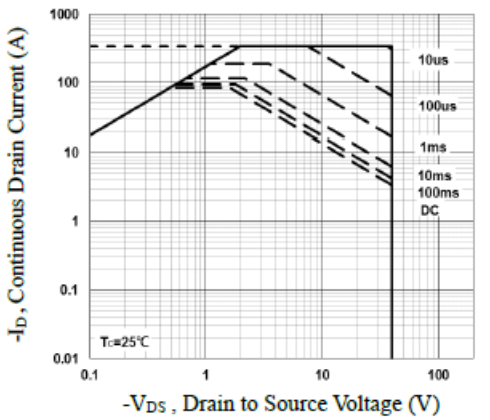


Fig.6 Maximum Safe Operation Area

TYPICAL CHARACTERISTICS

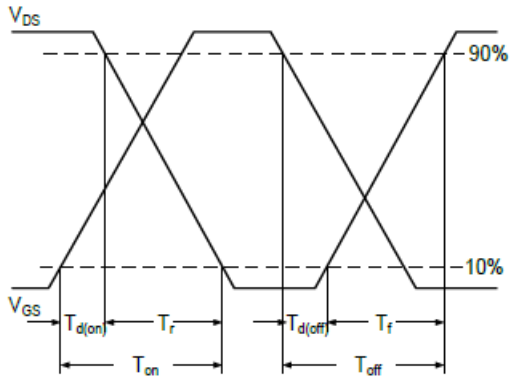


Fig.7 Switching Time Waveform

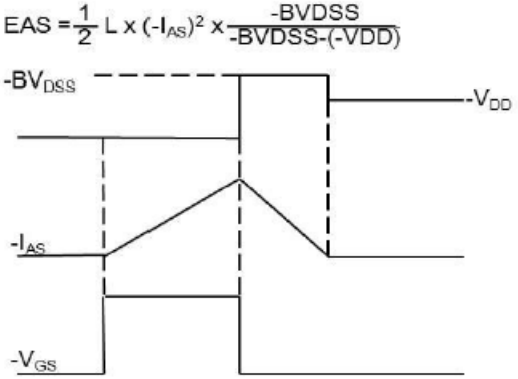


Fig.8 EAS Waveform

\

SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
© http://www.syncpower.com