



# SPP9433W

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP9433W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

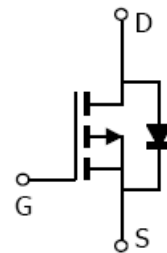
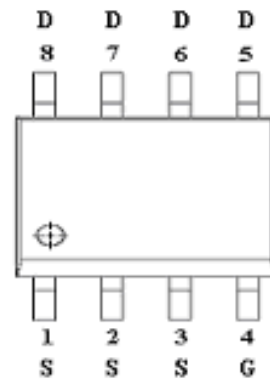
### FEATURES

- ◆ -30V/-6A,  $R_{DS(ON)}=42m\Omega@V_{GS}=-10V$
- ◆ -30V/-3A,  $R_{DS(ON)}=78m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8 package design

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

### PIN CONFIGURATION(SOP-8)



### PART MARKING



A : Lot Code  
B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9433WS8RGB	SOP-8	SPP9433W

※ SPP9433WS8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-30	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C	-6	A
		T <sub>A</sub> =70°C	-4	
Pulsed Drain Current	I <sub>DM</sub>	-12	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-6	A	
Power Dissipation	P <sub>D</sub>	2.08	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	60	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq -5V, V_{GS}=-10V$	-6			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-6A$		0.035	0.042	$\Omega$
		$V_{GS}=-4.5V, I_D=-3A$		0.065	0.078	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10.0V, I_D=-6A$		6		S
Diode Forward Voltage	$V_{SD}$	$I_S=-6A, V_{GS}=0V$			-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-6A$		6.4		nC
Gate-Source Charge	$Q_{gs}$			2.7		
Gate-Drain Charge	$Q_{gd}$			3.1		
Input Capacitance	$C_{iss}$	$V_{DS}=-24V, V_{GS}=0V$ $f=1MHz$		650		pF
Output Capacitance	$C_{oss}$			270		
Reverse Transfer Capacitance	$C_{rss}$			104		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-12V, I_D=-5.0A,$ $V_{GEN}=-10V$ $R_G=3.3\Omega$		9		nS
	$t_r$			16		
Turn-Off Time	$t_{d(off)}$			21		
	$t_f$			22		



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### TYPICAL CHARACTERISTICS

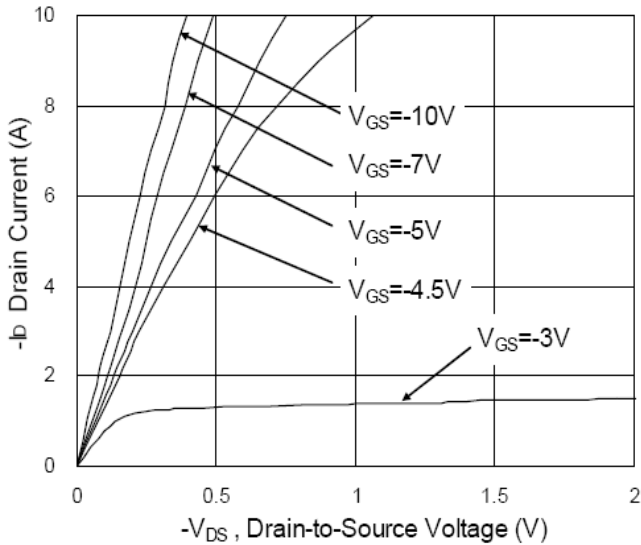


Fig. 1 Typical Output Characteristics

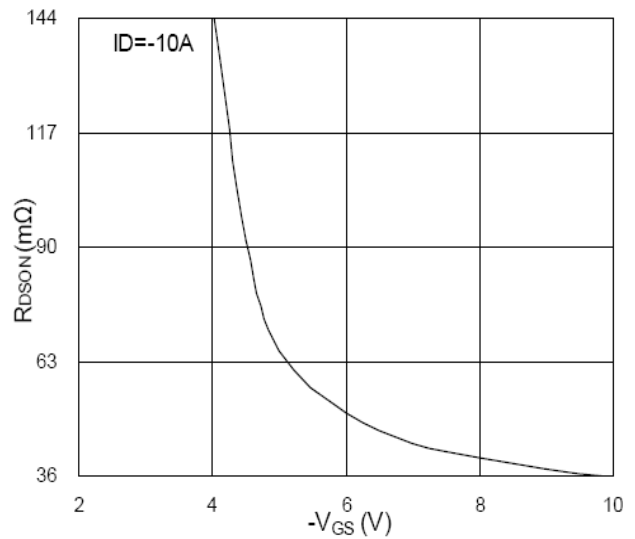


Fig. 2 On-Resistance vs. Gate Voltage

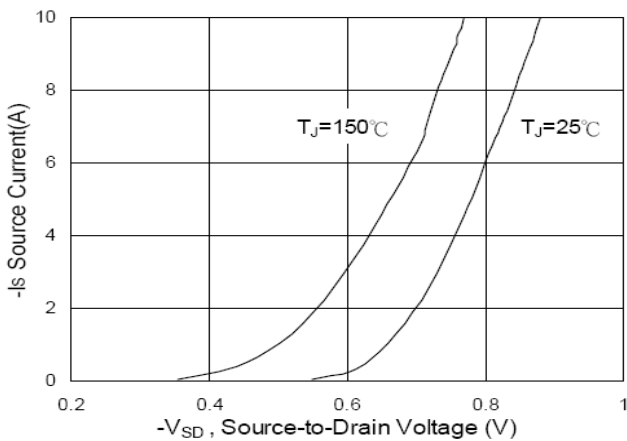


Fig. 3 Forward characteristics of Diodes

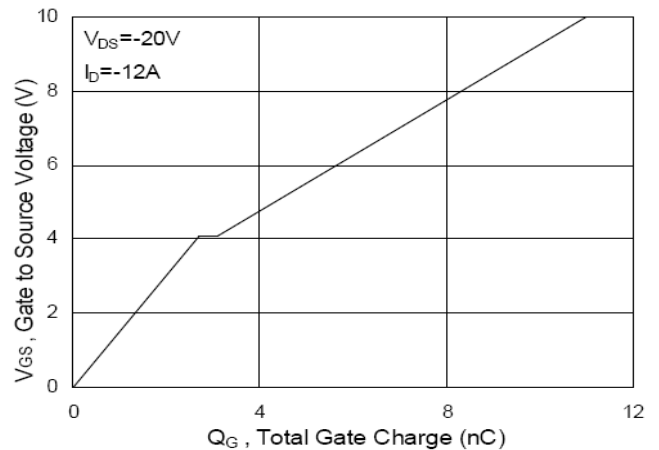


Fig. 4 Gate Charge Characteristics

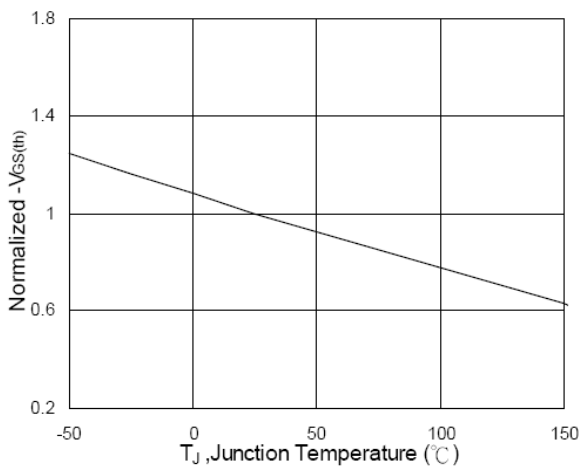


Fig. 5  $V_{GS}$  vs. Junction Temperature

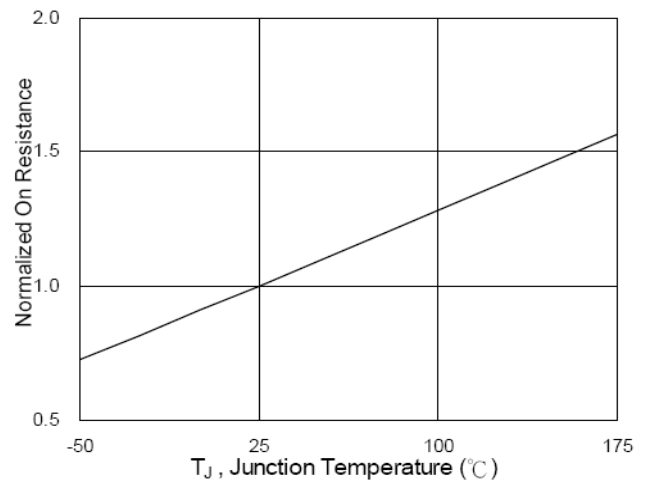


Fig. 6 On-Resistance vs Junction Temp



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## TYPICAL CHARACTERISTICS

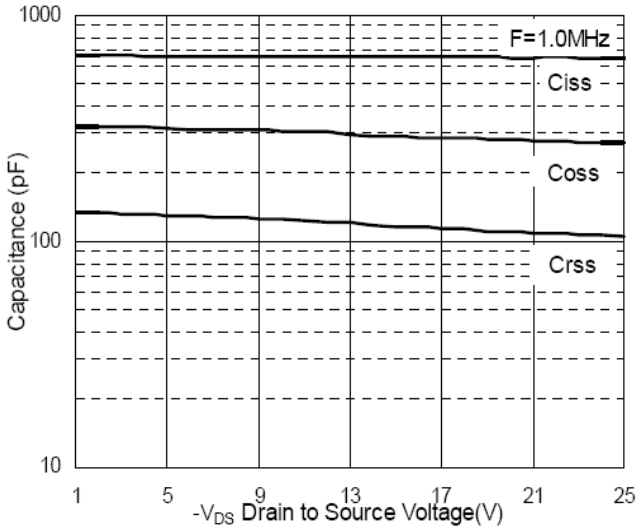


Fig. 7 Typical Capacitance Characteristics

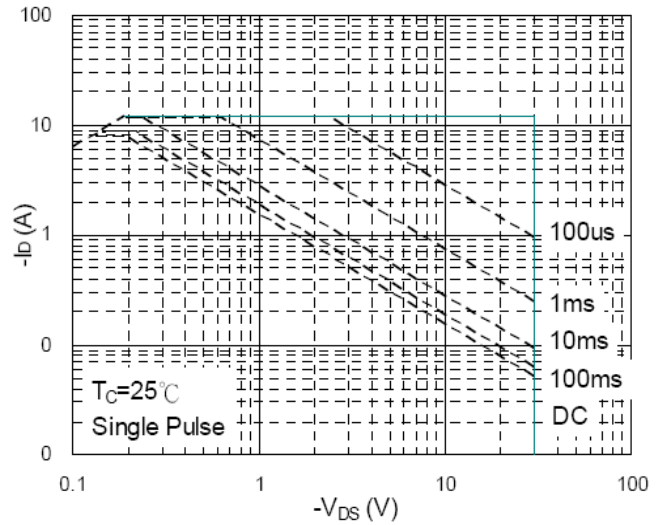


Fig. 8 Maximum Safe Operation Area

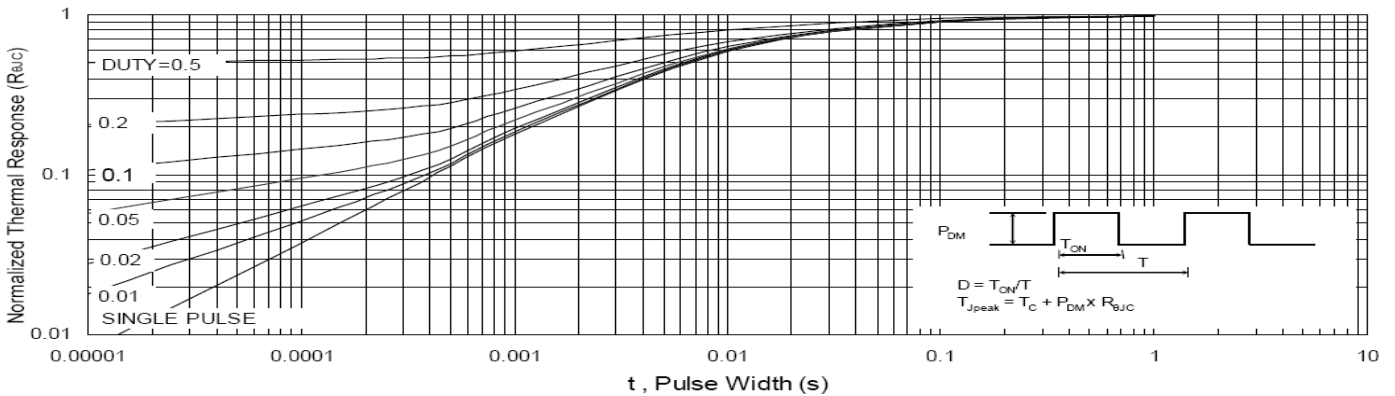


Fig. 9 Effective Transient Thermal Impedance

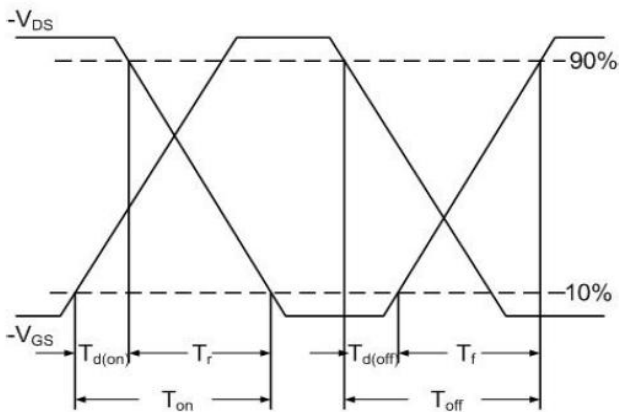


Fig. 10 Switching Time Waveform

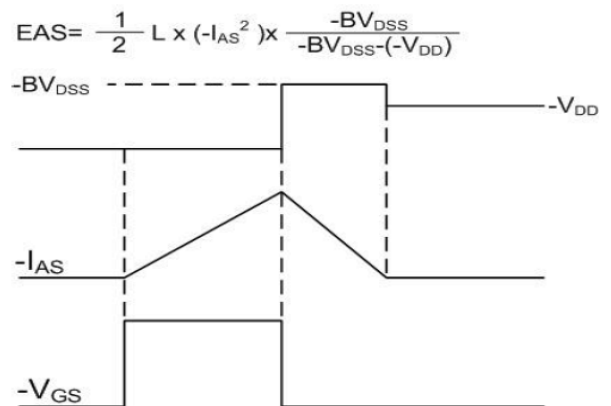


Fig. 11 Unclamped Inductive Waveform



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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