SPP9972
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP9972 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP9972 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

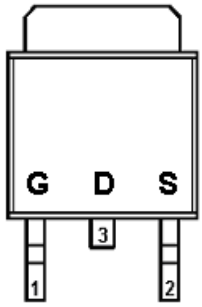
- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

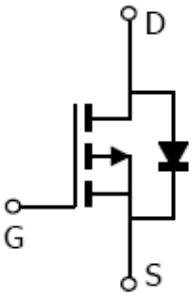
FEATURES

- -60V/-18A,$R_{DS(ON)}$= 25mΩ@V_{GS}=- 10V
- -60V/- 12A,$R_{DS(ON)}$= 33mΩ@V_{GS}=- 4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

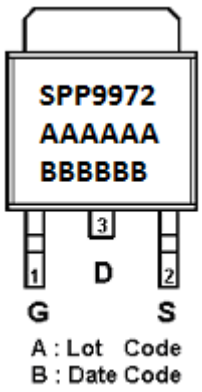
PIN CONFIGURATION

TO-252





PART MARKING



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9972T252RGB	TO-252	SPP9972

※ SPP9972T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-35	A
	T_A=100℃		-27	
Pulsed Drain Current		I_{DM}	-70	A
Single Pulse Avalanche Energy		EAS	162	mJ
Power Dissipation	T_A=25℃	P_D	52	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JC}$	2.4	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V			-1	uA
		V_{DS}=-48V,V_{GS}=0V T_J=55℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}= -0V,V_{GS} =-0V			-35	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D= -18A		0.02	0.025	Ω
		V_{GS}=-4.5V,I_D= -12A		0.026	0.033	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-18A		23		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS} =0V			-1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-20V,V_{GS}=-4.5V I_D= -12A		25		nC
Gate-Source Charge	Q_{gs}			6.7		
Gate-Drain Charge	Q_{gd}			5.5		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		3635		pF
Output Capacitance	C_{oss}			225		
Reverse Transfer Capacitance	C_{rss}			140		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,I_D=-1A, V_{GEN}=-10V, R_G=3.3Ω		38		nS
	t_r			24		
Turn-Off Time	$t_{d(off)}$			100		
	t_f			7		

TYPICAL CHARACTERISTICS

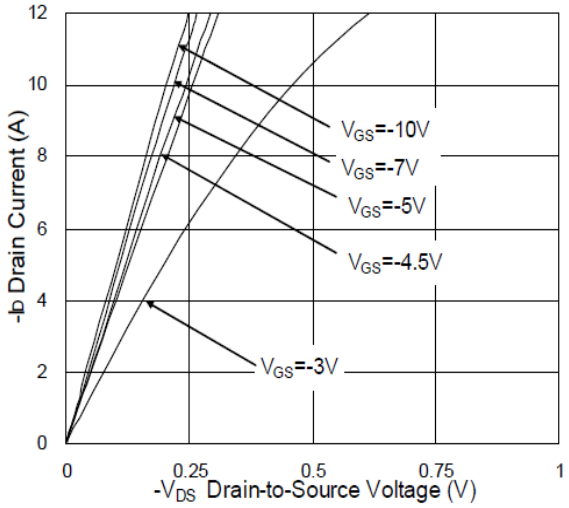

Fig 1. Output Characteristic

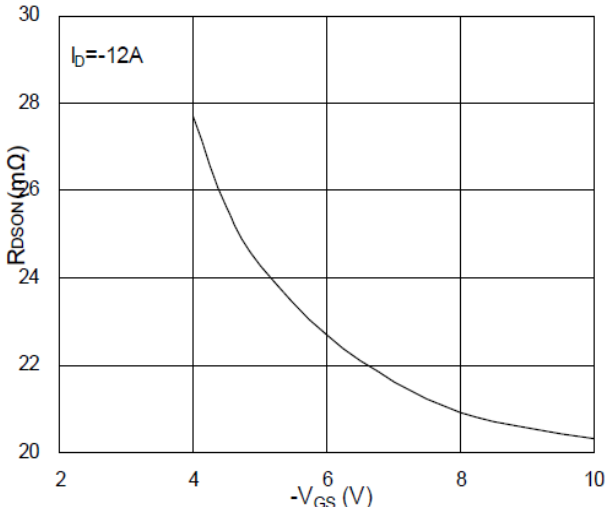

Fig 2. On Resistance vs Gate Source Voltage

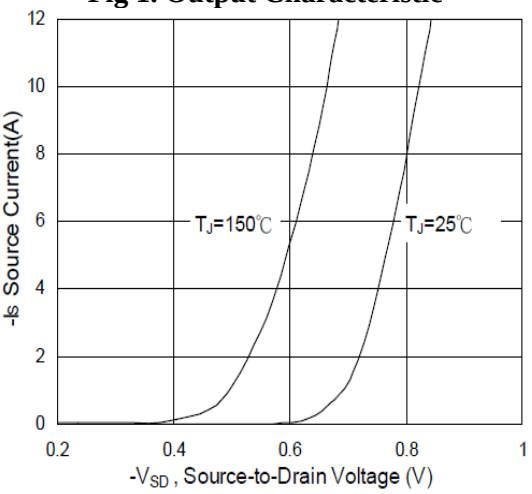

Fig 3. Source-Drain Diode Forward Voltage

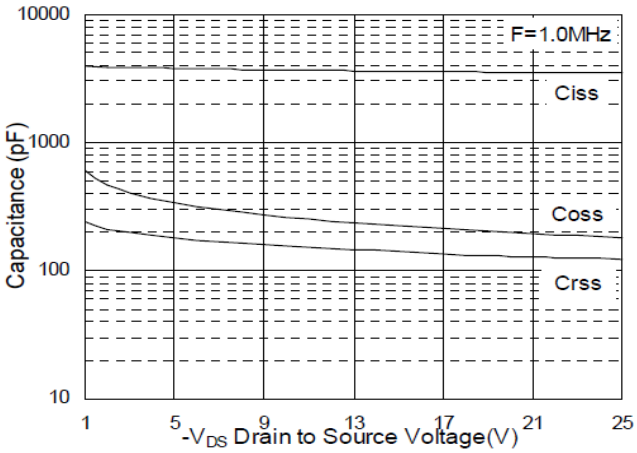

Fig 4. Capacitance

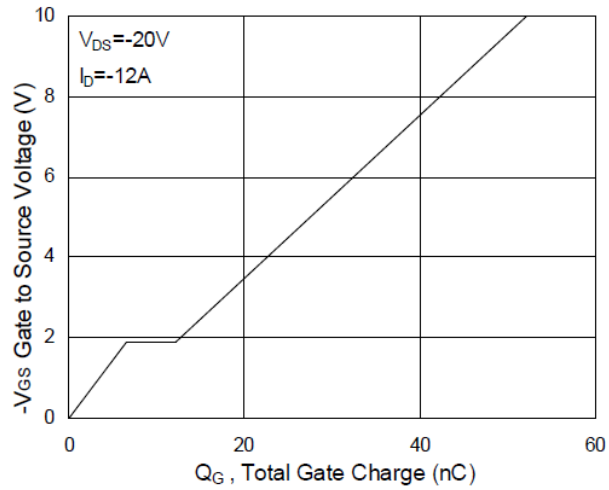

Fig 5. Gate Charge

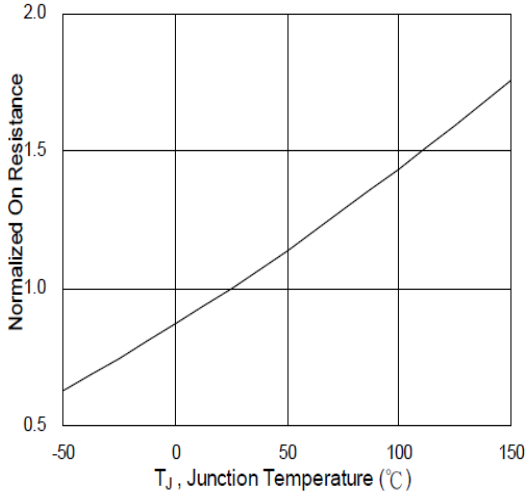

Fig. 6 On Resistance vs Junction Temperature

TYPICAL CHARACTERISTICS

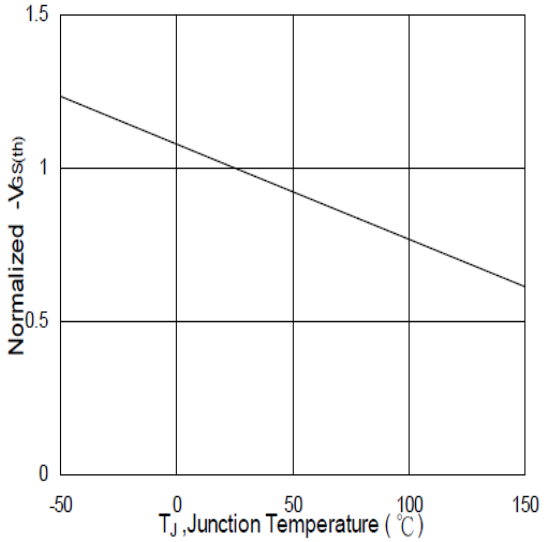

Fig. 7 Threshold Voltage vs Temperature

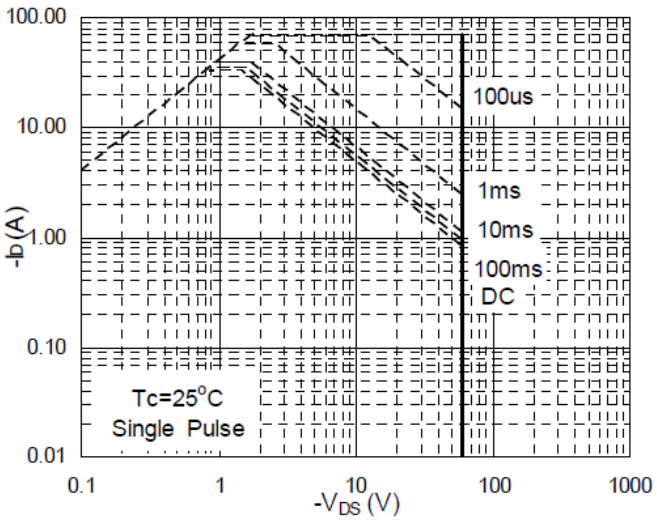

Fig. 8 Save Operating Rnage

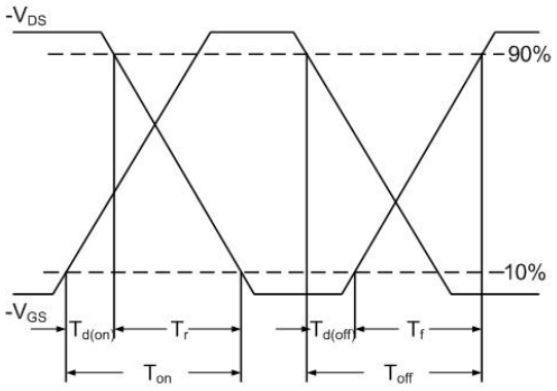

Fig 9. Switching Time Waveform

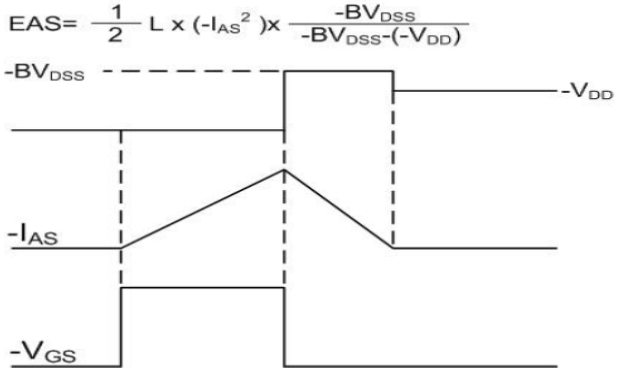

Fig. 10 Unclamped Inductive Waveform

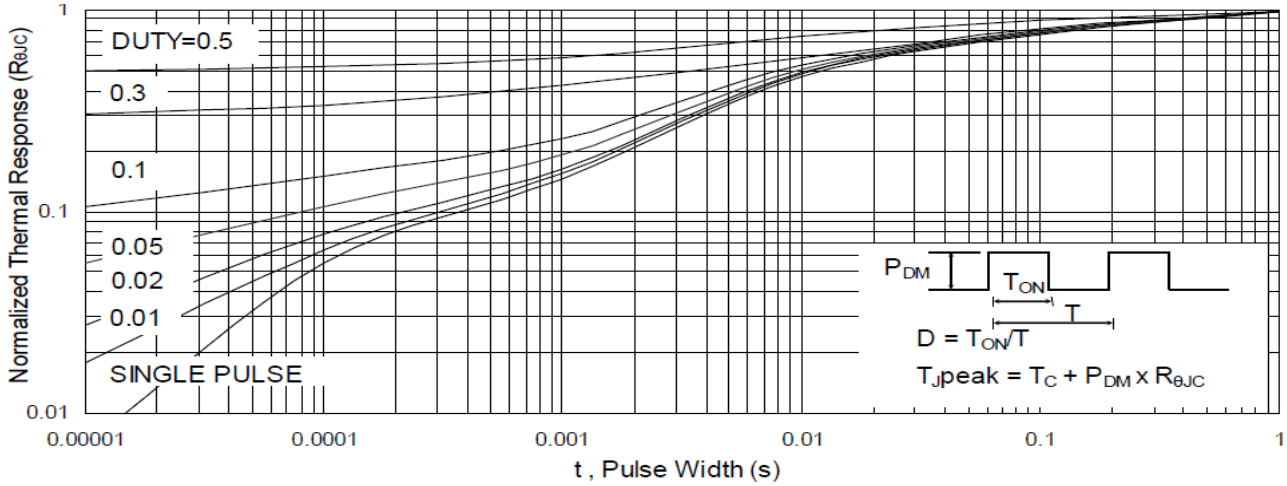

Fig 11. Maximum Transient Thermal Impedance

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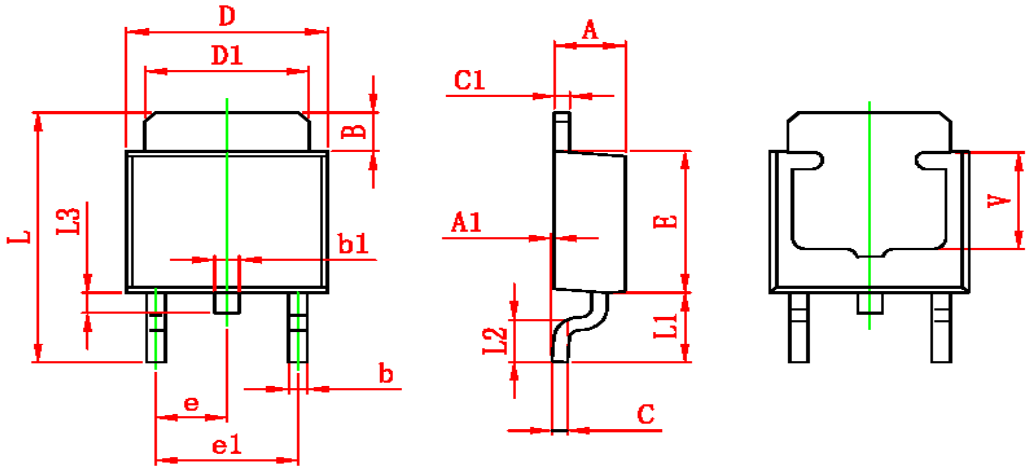
TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.350	0.650	0.014	0.026
V	3.80 REF		0.150 REF	

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